Internal Use Only

Service Manual

LG-A290

Date: January, 2012 / Issue 1.0

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.
The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. 

Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop
PAM	Power Amplifier Module

PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. SYSTEM SPECIFICATION

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Lithium Ion, 3.7V 1500mAh	
Stand by TIME	>450 hr., Min.@PP9	
Stand by time	>500 hr., Min.@PP5	
Talk time	>6.0hr., Min.@GSM900, PL=5 >14.0 hr., Min.@GSM900, PL=13 >8 hr., Min.@DCS, PL=0 >14 hr., Min.@DCS, PL=9	
Charging time	Approx. 3 hours 30 min.	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 32.3dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V Small	
Display	MAIN : TFT 176 × 220(QCIF) pixel 262K Color	
Status Indicator	KEY TOTAL 22EA Hard icons. Key Pad Numeric(12EA : 0 ~ 9, #, *) Navigation Key OK Key(5EA) Menu Key, Clear Key, Send Key, End Key, SIM Switch Key(5EA)	
ANT	Internal	
EAR Phone Jack	Yes(3.5Ø)	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	

Item	Feature	Comment
Microphone	Yes	
Speaker/Receiver	18 x 12 Speaker/Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	1.3M	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

<table>
<tr><th>Item</th><th>Description</th><th colspan="6">Specification</th></tr>
<tr><td>1</td><td>Frequency Band</td><td colspan="3">GSM850
TX: 824 ~ 849 MHz
RX: 869 ~ 894 MHz
DCS
TX: 1710 ~ 1785 MHz
RX: 1805 ~ 1880 MHz
PCS
TX: 1850 ~ 1910 MHz
RX: 1930 ~ 1990 MHz</td><td colspan="3">EGSM
TX: 880 ~ 915MHz
RX: 925 ~ 960 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td colspan="6">RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td colspan="6">< 0.1ppm</td></tr>
<tr><td rowspan="20">4</td><td rowspan="20">Power Level</td><td colspan="6">GSM850 / EGSM</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>5</td><td>33 dBm</td><td>±2dB</td><td>13</td><td>17 dBm</td><td>±3dB</td></tr>
<tr><td>6</td><td>31 dBm</td><td>±3dB</td><td>14</td><td>15 dBm</td><td>±3dB</td></tr>
<tr><td>7</td><td>29 dBm</td><td>±3dB</td><td>15</td><td>13 dBm</td><td>±3dB</td></tr>
<tr><td>8</td><td>27 dBm</td><td>±3dB</td><td>16</td><td>11 dBm</td><td>±5dB</td></tr>
<tr><td>9</td><td>25 dBm</td><td>±3dB</td><td>17</td><td>9 dBm</td><td>±5dB</td></tr>
<tr><td>10</td><td>23 dBm</td><td>±3dB</td><td>18</td><td>7 dBm</td><td>±5dB</td></tr>
<tr><td>11</td><td>21 dBm</td><td>±3dB</td><td>19</td><td>5 dBm</td><td>±5dB</td></tr>
<tr><td>12</td><td>19 dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
<tr><td colspan="6">DCS / PCS</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>0</td><td>30 dBm</td><td>±2dB</td><td>8</td><td>14 dBm</td><td>±3dB</td></tr>
<tr><td>1</td><td>28 dBm</td><td>±3dB</td><td>9</td><td>12 dBm</td><td>±4dB</td></tr>
<tr><td>2</td><td>26 dBm</td><td>±3dB</td><td>10</td><td>10 dBm</td><td>±4dB</td></tr>
<tr><td>3</td><td>24 dBm</td><td>±3dB</td><td>11</td><td>8 dBm</td><td>±4dB</td></tr>
<tr><td>4</td><td>22 dBm</td><td>±3dB</td><td>12</td><td>6 dBm</td><td>±4dB</td></tr>
<tr><td>5</td><td>20 dBm</td><td>±3dB</td><td>13</td><td>4 dBm</td><td>±4dB</td></tr>
<tr><td>6</td><td>18 dBm</td><td>±3dB</td><td>14</td><td>2 dBm</td><td>±5dB</td></tr>
<tr><td>7</td><td>16 dBm</td><td>±3dB</td><td>15</td><td>0 dBm</td><td>±5dB</td></tr>
</table>

Item	Description	Specification	
5	Output RF Spectrum (due to modulation	**GSM850 / EGSM**	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ <1,200	-60
		1,200 ~ <1,800	-60
		1,800 ~ <3,000	-63
		3,000 ~ <6,000	-65
		6,000	-71
		DCS/ PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ <1,200	-60
		1,200 ~ <1,800	-60
		1,800 ~ <3,000	-65
		3,000 ~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	**GSM850 / EGSM**	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Output RF Spectrum
(due to switching transient)</td><td colspan="3">DCS/ PCS</td></tr>
<tr><td>Offset from Carrier (kHz).</td><td colspan="2">Max. dBm</td></tr>
<tr><td>400</td><td colspan="2">-22</td></tr>
<tr><td>600</td><td colspan="2">-24</td></tr>
<tr><td>1,200</td><td colspan="2">-24</td></tr>
<tr><td>1,800</td><td colspan="2">-27</td></tr>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850, EGSM
BER (Class II) < 2.439% @-102 dBm
DCS,PCS
BER (Class II) < 2.439% @-102 dBm</td></tr>
<tr><td>9</td><td>RX Level Report Accuracy</td><td colspan="3">± 3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">15±3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>-</td></tr>
<tr><td>12</td><td>RLR(Norminal)</td><td colspan="2">4± 3 dB</td><td></td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="11">13</td><td rowspan="11">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-6</td><td>-</td></tr>
<tr><td>200</td><td>2</td><td>-</td></tr>
<tr><td>300</td><td>2</td><td>-9</td></tr>
<tr><td>500</td><td>*</td><td>*</td></tr>
<tr><td>1,000</td><td>2</td><td>-7</td></tr>
<tr><td>3,000</td><td>2</td><td>*</td></tr>
<tr><td>3,400</td><td>2</td><td>-12</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR(Vol. Nominal)</td><td colspan="3">>17dB</td></tr>
<tr><td>15</td><td>Echo Loss</td><td colspan="3">>58dB</td></tr>
<tr><td>16</td><td>Idle Noise Sending</td><td colspan="3">< -64dBm0p</td></tr>
<tr><td>17</td><td>Idle Noise Receiving</td><td colspan="3">< -54dBm0P(Volume Max)</td></tr>
<tr><td>18</td><td>System frequency
(13 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
<tr><td>19</td><td>32.768KHz tolerance</td><td colspan="3">≤ 30 ppm</td></tr>
<tr><td>20</td><td>Ringer Volume</td><td colspan="3">At least 58 dB spl under below conditions:
1. Ringer set as ringer.
2. Test distance set as 100 cm</td></tr>
<tr><td>21</td><td>Charge Current</td><td colspan="3">Fast Charge : Typ. 600 mA
Slow Charge : Typ. 500mA
Total Charging Time : < Approx. 3 hours 30min.</td></tr>
</table>

Item	Description	Specification	
22	Antenna Display	Bar Number	Power
		4	over -91dBm±2dBm
		4 -> 3	-91dBm±2dBm
		3 -> 2	-99dBm±2dBm
		2 -> 1	-103dBm±2dBm
		1 -> 0	-105dBm±2dBm
23	Battery Indicator	Battery Bar Number	Voltage
		3	≥ 3.75± 0.05 V
		3 -> 2	3.75 ± 0.05 V
		2 -> 1	3.65 ± 0.05 V
		1 -> 0	3.5 ± 0.05 V
24	Low Voltage Warning (Blinking Bar)	≤ 3.5 ± 0.05V (Call), every 1 minute	
		≤ 3.5 ± 0.05V (Standby), every 3 minute.	
25	Forced shut down Voltage	3.35 ± 0.05V	
26	Sustain RTC without battery	Over 1 min(Super Cap : Polyacene Capacitor 10uAh)	
27	Battery Type	Li-Ion Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 1500mAh	
28	Travel Charger	Switching-mode charger Input: 90 ~ 264 V, 47/63 Hz Output: 5.1 V, 700 mA	

3. TECHNICAL BRIEF

3.1 Digital Main Processor

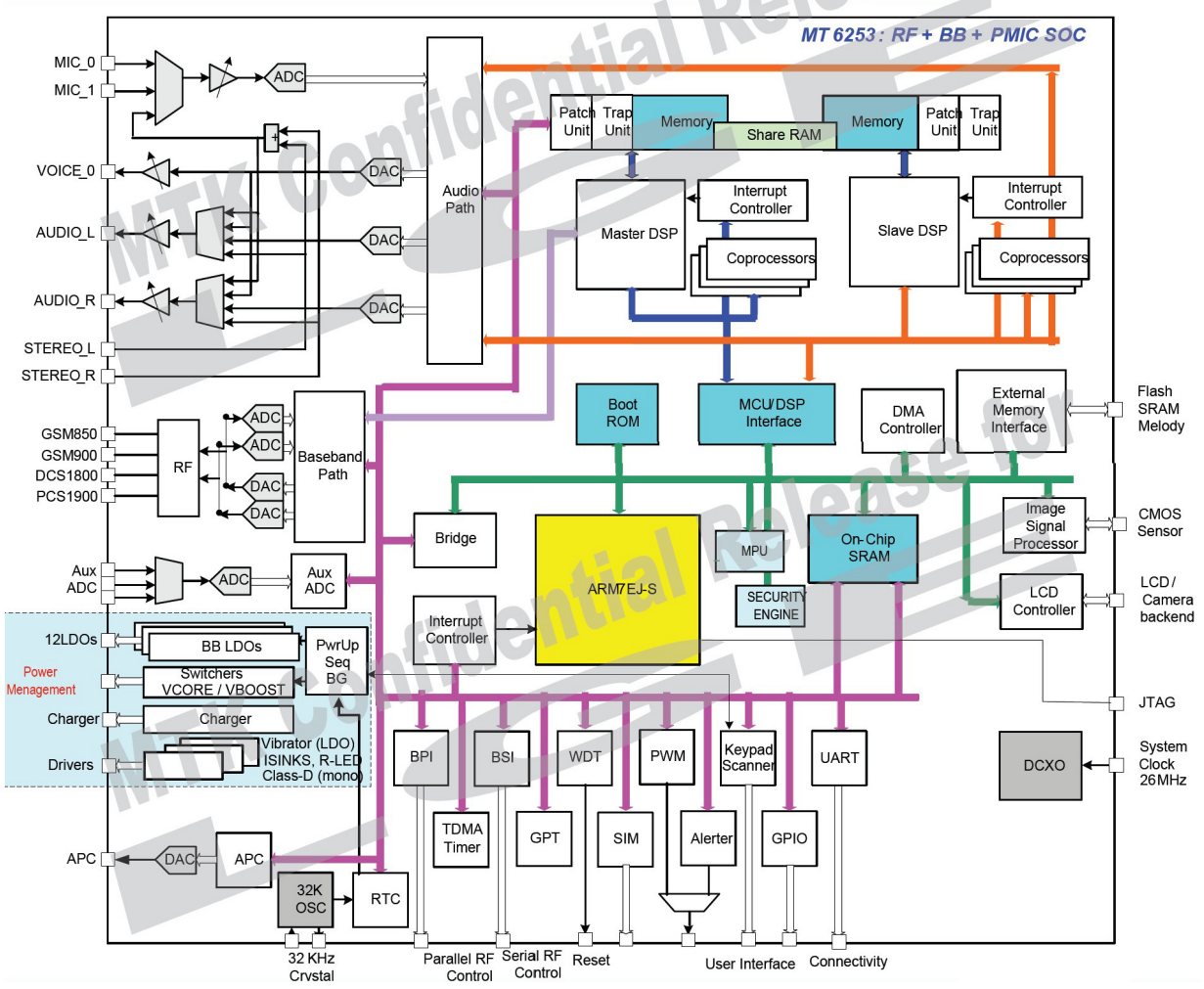


Figure. 3.1.1 MT6253 Hardware Block Diagram

3.1.1 General

• Integrated voice-band, audio-band and base-band analog front ends.
• Package:
  – aQFN, 11.5x11.5x0.85 mm.
  – 0.47 mm pitch.
  – 260balls, 0.47mm pitch package.

3.1.2 MCU Subsystem

• ARM7EJ-S 32-bit RISC processor.
• High performance multi-layer AMBA bus.
• Operating frequency 52/104MHz.
• Dedicated DMA bus, 7DMA channels.
• 144KB 0n-chip SRAM.
• On-chip boot ROM for Factory Flash Programming.
• Watchdog timer for system crash recovery.
• 3 sets of General Purpose Timer.
• Circuit Switch Data coprocessor.
• Division coprocessor.

3.1.3 External Memory Interface

• Supports up to 3 external devices.
• Supports 16-bit memory components with maximum size of up to 64M Bytes for each bank.
• Supports Flash and SRAM/PSRAM with Burst Mode.
• Support legacy industry standard parallel LCD Interface.
• Suppport multi-media companion chips with 8/16 bits data width.
• Configurable driving strength for memory interface.

3.1.4 User Interface

• 6-row x 7-column keypad control with hardware scanner.
• Support multi key press for gaming.
• SIM/USIM Controller with hardware T=0/T=1 protocol control.
• Real Time Clock(RTC) operating with a separate power supply.
• General Purpose I/Os (GPIOs).
• 1 set of Pulse Width Modulation(PWM) Output.
• Alerter Output with Enhanced PWM or PDM.
• Maximum 7 external interrupt lines.

3.1.5 Security

• Support security key and 128bit chip unique ID.

3.1.6 Connectivity

• 3 sets of UART with hardware flow control and speed up to 921600 bps.
• IrDA modulator/demodulator with hardware framer supports SIR mode of operation.
• HS/FS/LS USB 2.0 Device controller.
• Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Prto/SDIO host controller.
• Supports SDIO interface for SDIO peripherals as well as WIFI connectivity.
• DAI/PCM and !2S interface for Audio application.

3.1.7 Low Power Schemes

• Power Down Mode for analog and digital circuits.
• Processor Sleep Mode.
• Pause Mode of 32KHs clocking at Standby State.
• 3-channel Auxiliary 10-bit A/D Converter for application usage other than battery monitoring.

3.1.8 Power and Supply Management

• 2.8V to 4.7V Input Range.
• Charger Input up to 8V.
• 11 sets of LDO Optimized Specific GSM Sub-systems.
• One LDO for RF transceiver.
• High Operation Efficiency and Low Stand-by Current.
• Dual SIM Card Interface.
• One boost regulator and Four Open-Drain Output Current Regulators to Supply/Control the LED.
• LDO type Vibrator.
• One NMOS switch to control R(GB) LED.
• Thermal Overload Protection.
• Under Voltage Lock-out Protection.
• Over Voltage Protection.

3.1.9 Integrated RF Receiver

• Direct conversion architecture.
• Quad band differential input LNAs.
• Quadrature RF mixers.
• Fully integrated channel filter with f3dB=150kHs.
• 95dB gain with 60dB gain control range.
• No IIP2 calibration.

3.1.10 Integrated RF Transmitter

- Offset phase lock loop.
- IQ modulator DC offset calibration by BB ADC/DAC.
- Precise quadrature by IF divide-by-4.
- Integrated loop filter.

3.1.11 Integrated RF Frequency Synthesizer

- Programmable fractional-N synthesizer.
- Integrated wide range RFVCO.
- Integrated loop filter.
- Fast setting time suitable for multi-slot SPRS applications.

3.1.12 Integrated RF Digitally-Controlled Crystal Oscillator(DCXO)

- One-pin 26MHz crystal oscillator.
- On-chip programmable capacitor array for cross tune.

3.1.13 Radio Interface and Baseband Front End

- GMSK modulator with analog I and Q channel outputs.
- 10-bit D/A Converter for uplink baseband I and Q signals.
- 14-bit high resolution A/D Converter for downlink baseband I and Q signals.
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter.
- 10-bit D/A Converter for Automatic Power Control.
- Programmable Radio RX filter with adaptive bandwidth control.
- Dedicated Rx filter for FB acquisition.
- 6-Pin Baseband Parallel Interface(BRI) with programmable driving strength.
- Multi-band support.

3.1.14 Voice and Modem CODEC

- Digital tone generation.
- Voice Memo.
- Noise Reduction.
- Echo Suppression.
- Advanced Sidetone Oscillation Reduction.
- Digital sidetone generator with programmable gain.
- Two programmable acoustic compensation filters.
- GSM/GPRS quad vocoders for adaptive multirate(AMR), enhanced full rate(EFR), full. rate(FR), and half rate(HR).
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering.
- GPRS GEA1, GEA2 and GEA3 ciphering.

3.1.15 Voice Interface and Voice Front End

- Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control(AGC) mechanism.
- Voice power amplifier with programmable gain.
- 2nd order Sigma-delta A/D Converter for voice uplink path.
- D/A Converter for voice downlink path.
- Supporter for voice downlink path.
- Supports half-duplex hands-free operation.
- Compliant with GSM 03.05

3.1.16 LCD Interface

- Dedicated Parallel Interface supports 2 external 8/9 bit Parallel Interface, and Serial interface for LCM.

3.1.17 LCD Controller

- Supports LCM format: RGB332, RGB444, RGB565, RGB666, RGB888.
- Supports LCD module with maximum resolution up to 240x320 at 16bpp.
- Capable of combining display memories with up to 4 blending layers.
- Accelerated Gamma correction with programmable gamma table.
- Supports hardware display rotation for each layer.

3.1.18 Audio CODEC

- Wavetable synthesis with up to 64 tones.
- Advanced wavetable synthesizer capable of generating and 47 sets of percussions.
- PCM Playback and Record.
- Digital Audio Playback.

3.1.19 Audio Interface and Audio Front End

- Supports I2S interface.
- High resolution D/A Converters for Stereo Audio playback.
- Stereo analog input for stereo audio source.
- Analog multiplexer for Stereo Audio.
- FM Radio Recording.
- Stereo to Mono Conversion.
- HE-AAC decode support.

3.2 Power Management

Power management unit, so called PMU, is integrated into analog part. To facilitate software control and interface design, PMU control share the CCI interface along with other analog parts, such as BBTX, BBRX, VBI and ABI during FT.

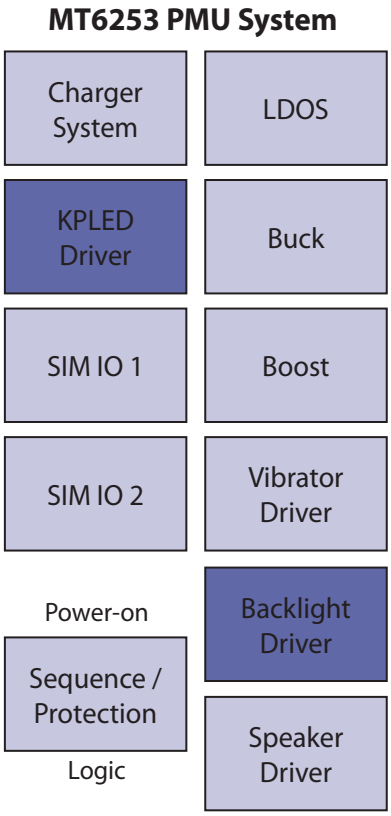


Figure. 3.2.1 PMU system block diagram

3.2.1 Low Dropout Regulators(LDOs), Buck converterand Reference

The PMU Integrates 12 LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, and output noise.

■ RF LDO (Vrf)

The RF LDO is a linear regulator that could source 180mA (max) with 2.8V output voltage. It supplies the RF circuitry of the handset. The LDO is optimized for high performance and adequate quiescent current.

■ **Digital Core Buck Converter (Vcore)**

The digital core regulator is a DC-DC step-down (Buck converter) that could source 200mA(max) with 1.2V to 0.9V programmable output voltage based on software register setting. It supplies the power for baseband circuitry of the SoC. The buck converter is optimized for high efficiency and low quiescent current.

■ **Digital IO LDO (Vio)**

The digital IO LDO is a linear regulator that could source 100mA (max) with 2.8V output voltage. It supplies the the power for baseband circuitry of the SoC. The LDO is optimized for very low quiescent current and turns on automatically together with Vm/Va LDOs.

■ **Analog LDO (Va)**

The analog LDO is a linear regulator that could source 100mA (max) with 2.8V output voltage.
It supplies the analog sections of the SoC. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the burst at 217Hz of RF power amplifier.

■ **TCXO LDO (Vtcxo)**

The TCXO LDO is a linear regulator that could source 20mA (max) with 2.8V output voltage.
It supplies the temperature compensated crystal oscillator, which needs ultra low noise supply with very good ripple rejection.

■ **Single-Step RTC LDO (Vrtc)**

The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell to 2.8V, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features the reverse current protection and is optimized for ultra low quiescent current while sustaining the RTC function as long as possible.

■ **Memory LDO (Vm)**

The memory LDO is a linear regulator that could source 200mA (max) with 1.8V or 2.8V output voltage selection based on the supply specification of memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current with wide output loading range.

■ **SIM LDO (Vsim)**

The SIM LDO is a linear regulator that could source 80mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules (SIM) card. It supplies the SIM card and SIM level shifter circuitry in the handset. The Vsim LDO is controlled independently by the register named VSIM_EN.

■ **SIM2 LDO (Vsim2)**

The SIM2 LDO is a linear regulator that could source 20mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of the 2nd subscriber identity modules (SIM) card.
It supplies the 2nd SIM card and SIM level shifter circuitry in the handset. The Vsim2 LDO is controlled independently by the register named VSIM2_EN.

■ **USB LDO (Vusb)**

The USB LDO is a linear regulator that could source 75mA (max) with 3.3V output dedicated for USB circuitry. It is controlled independently by the register named RG_VUSB_EN.

■ **Memory Card / Bluetooth LDO (Vbt)**

The VBT LDO is a linear regulator that could source 150mA (max) with 1.5V, 1.8V, 2.5V or 2.8V output for memory card or Bluetooth module. It is controlled independently by the register named RG_VBT_EN.

■ **Camera Analog LDO (Vcama)**

The Vcama LDO is a linear regulator that could source 150mA (max) with 1.5V, 1.8V, 2.5V or 2.8V output which is selected by the register named VCAMA_SEL[1:0]. It supplies the analog power of the camera module. Vcama is controlled independently by the register named RG_VCAMA_EN.

■ **Camera Digital LDO (Vcamd)**

The Vcamd LDO is a linear regulator that could source 75mA (max) with 1.3V, 1.5V, 1.8V or 2.8V output which is selected by the register named VCAMD_SEL[1:0]. It supplies the digital power of the camera module. Vcamd is controlled independently by the register named RG_VCAMD_EN.

VCORE	1V2 / 1V0	200 mA	PMU (BB)
VIO	2V8	100 mA	PULL UP(I2C1, I2C2, BT_PCMSYNC, BAT CONNECTOR) SIM Selection, Jack DET, Hook DET, LCD, FM Radio
VRF	2V8	200 mA	PAM
VA	2V8	125 mA	BB(PLL, RFE, MBUF, AFE, RFD)
VM	1V8 / 2V8	200 mA	EMI (BB), MEMORY
VTCXO	2V8	20 mA	DCXO (BB)
VSIM	1V8 / 3V0	80 mA	SIM1
VSIM2	1V8 / 3V0	20 mA	SIM2, SIM3
VUSB	3V3	100 mA	USB Power (BB)
VBT(VMMC)	1V8 / 2V84 / 3V0	150 mA	MSDC (BB), T-FLASH
VCAM_A	1V5 / 1V8 / 2V5 / 2V8	150 mA	CAMERA (ANALOG, IO)
VCAM_D	1V5 / 1V8 / 2V5 / 2V8	75 mA	CAMERA (DIGITAL)
VRTC	2V8	1 mA	

Table3.2.1. Power Supply Domains (Without RF)

3.2.1 Power On

Together with Power Management IC (PMIC), MT6253 offers both fine and coarse resolutions of power control through software programming. With this efficient method, the developer can turn on selective resources accordingly in order to achieve optimized power consumption. The operating modes of MT6253 as well as main power states provided by the PMIC are shown in Figure.3.2.1.

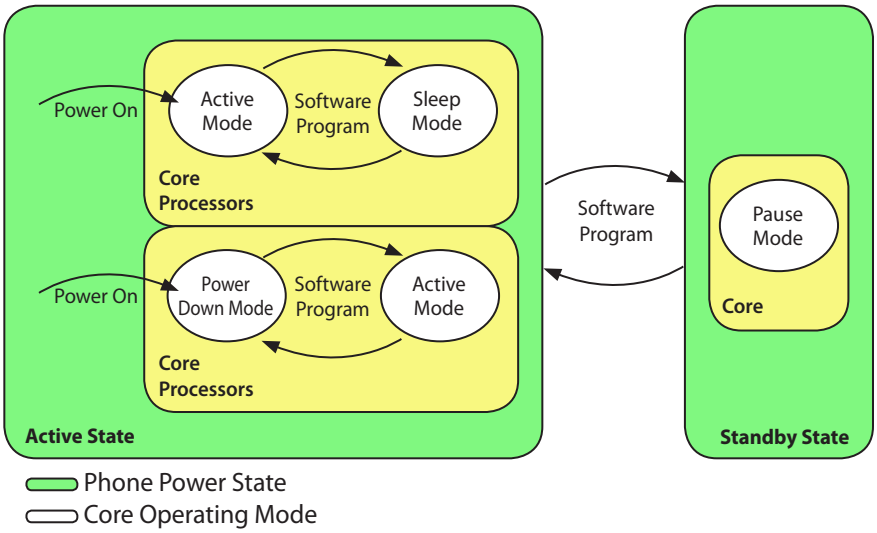


Figure 3.2.1. Major Phone Power States and Operating Modes for MT6253 based terminal

3.3 FEM with integrated Power Amplifier Module (SKY77550, U400)

3.3.1 Internal Block Diagram

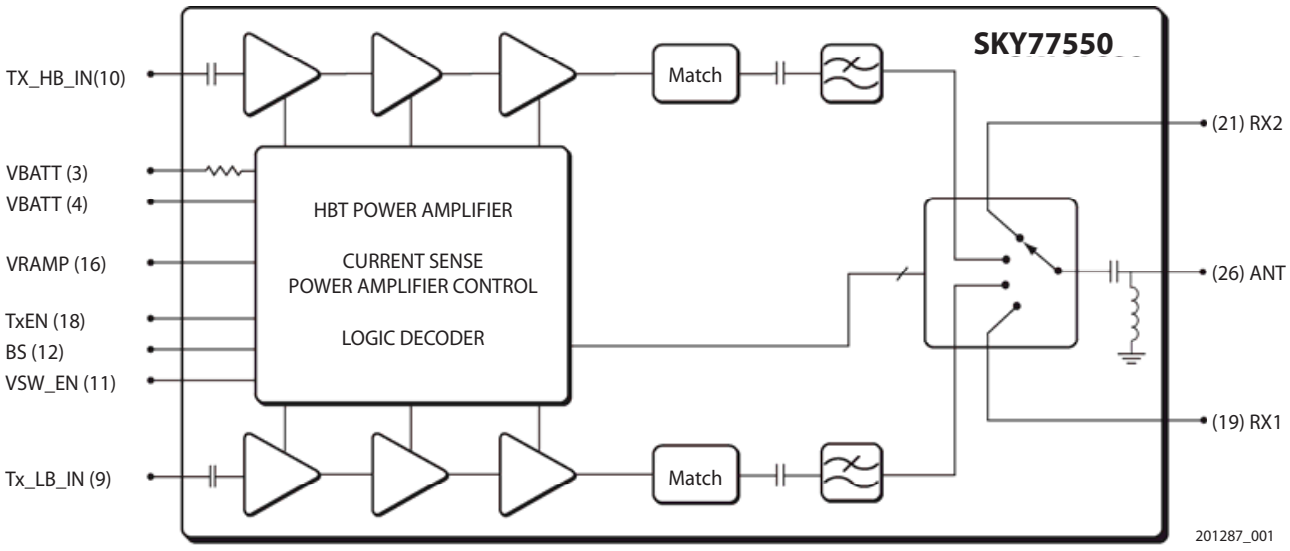


Figure. 3.3.1 SKY77550 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

SKY77550 is a transmit and receive Front-End Module (FEM) with Integrated Power Amplifier Control(iPAC™) for Dual-band cellular handsets comprising GSM850/900 and DCS1800/PCS1900 operation. Designed in a low profile, compact form factor, the SKY77550 offers a complete Transmit VCO-to-Antenna and Antenna-to-Receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of a GSM850/900 PA block and a DCS1800/PCS1900 PA block, impedance matching circuitry for 50 ohm input and output impedances, Tx harmonics filtering, high linearity / low insertion loss RF switch, and a Power Amplifier Control (PAC) block with internal current sense resistor. The two Hetero-junction Bipolar Transistor (HBT) PA blocks, a Bi-FET PAC and switch control circuit are fabricated onto a single Gallium Arsenide (GaAs) die. One PA block supports the GSM850/900 bands and the other PA block supports the DCS1800/PCS1900 bands.

Both PA blocks share common power supply pads to distribute current. The output of each PA block and the outputs to the two receive pads are connected to the antenna pad through an RF switch. The GaAs die, Switch die and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic over mold.

Mode	Input Contrpol Bits		
	VSW_EN	Tx_EN	BS
STANDBY	0	0	0
Rx1[1]	1	0	0
Rx2[1]	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

[1] Rx1 and Rx2 are broadband receive ports and each supports the GSM850, GSM900, DCS, and PCS nands.

Table 3.3.1 SKY77550 Mode Control Logic

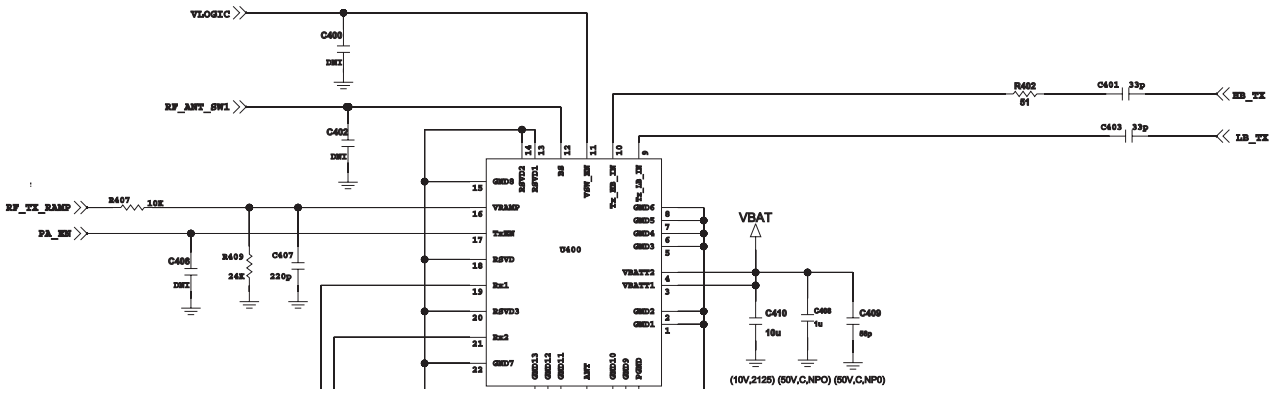


Figure 3.3.2 TX-module CIRCUIT DIAGRAM

3.4 Clocks

There are two major time bases in the MT6253. For the faster one is the 26 MHz clock originated from the digital control oscillator(DCXO) of RF block. This is then converted to the square-wave signal through CLKSQ.
The other time base is the 32768 Hz clock generated by an on-chip oscillator connected to an external crystal.

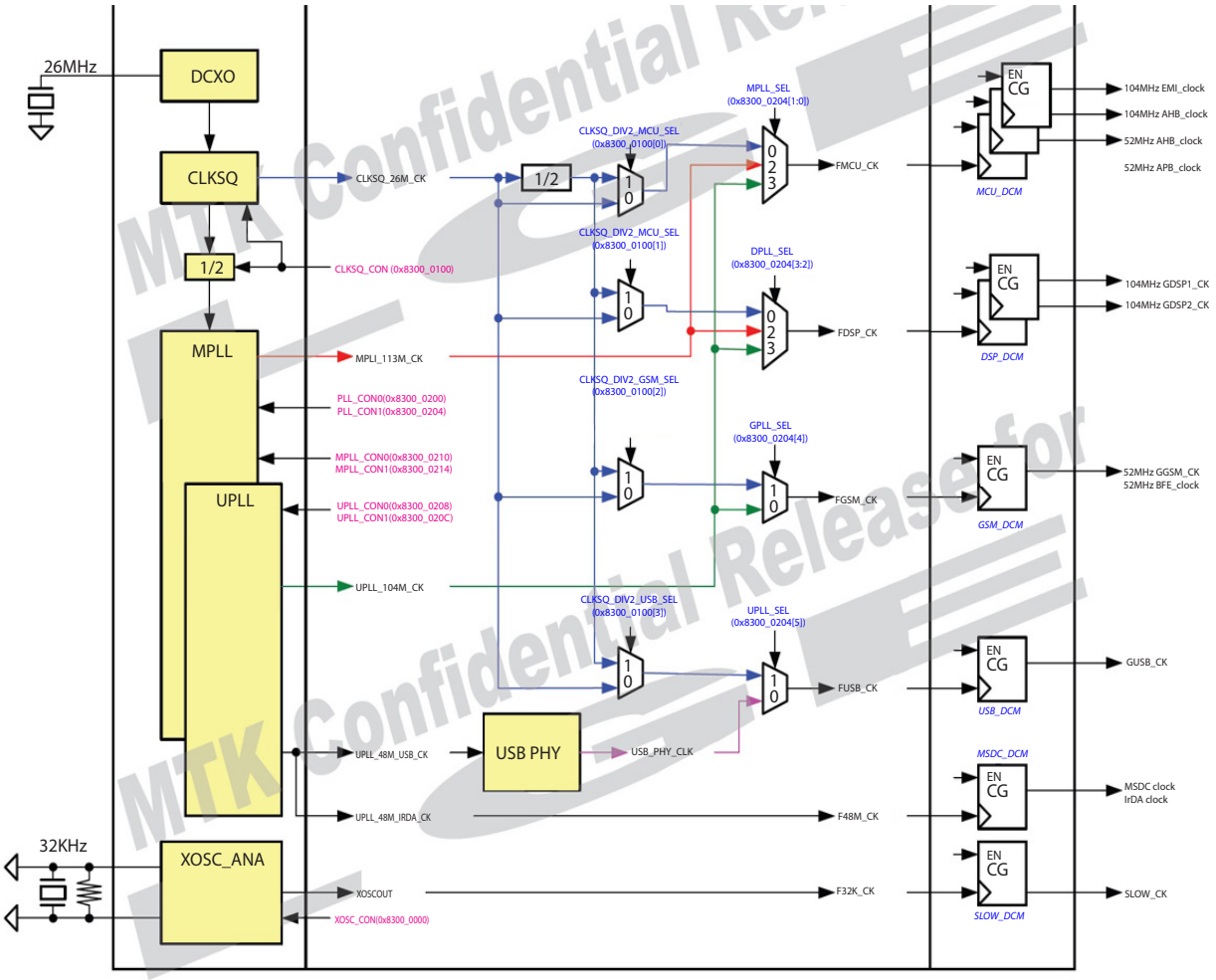


Figure. 3.4.1 Clock distributions inside the MT6253.

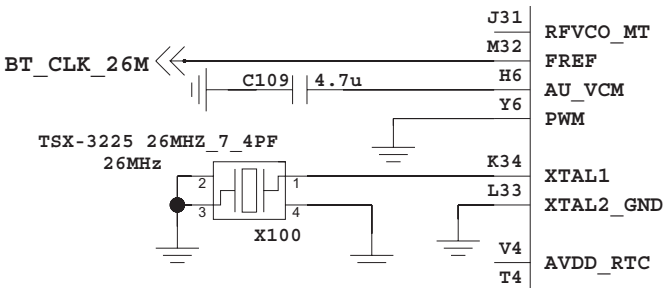


Figure. 3.4.2 Crystal Oscillator External Connection

3.4.1 32.768KHz Time Base

The 32768 Hz clock is always running. It's mainly used as the time base of the Real Time Clock(RTC) module, which maintains time and date with counters. Therefore, both the 32768Hz oscillator and the RTC module is powered by separate voltage supplies that shall not be powered down when the other supplies do.
In low power mode, the 13Mhz time base is turned off, so the 32768Hz clock shall be employed to update the critical TDMA timer and Watchdog Timer. This time base is also used to clocks the keypad scanner logic

3.4.2 26MHz Time Base

Since PLL are based on 13MHz reference clock. There is an ½-dividers for PLL existing to allow using 26MHz DCXO.
There are 2 phase-locked loops(PLL) in MT6253. The UPLL generates 624Mhz clock output, then a frequency divider further divide 6, and 13 to generate fixed 103Mhz, and 48Mhz for GSM_CLOCK and USB_CLOCK and DSP_CLOCK. These four primary clocks then feed into GSM, USB, MCU and DSP Clock Domain, respectively.
These 2 PLLs require no off-chip components for operations and can be turn off in order to save power. After power-on, the PLLs are off by default and the source clock signal is selected through multiplexers. The software shall take cares of the PLL lock time while changing the clock selections. The PLL and usages are listed below.
- PLL supply four clock source : MCU_CLOCK(104~113Mhz), DSP_CLOCK(104~113Mhz), GSM_CLOCK(104Mhz) and USB_CLOCK(48Mhz)
- For DSP/MCU system clock, MCU_CLOCK and DSP_CLOCK. The outputted 104~113Mhz clock is controlled by MCU for 500Khz per step and settled time is under 100uS. The clock is also connected to DSP/MCU DCM (dynamic clock manager) for dynamically adjusting clock rate by digital clock divider.
MCU_CLOCK paces the operations of the MCU cores, MCU memory system, and MCU peripherals as well
Modem system clock, GSM_CLOCK, which paces the operations of the GSM/GPRS hardware, coprocessors as well. The outputted 104Mhz clock is connecter to GSM_DCM for dynamically adjusting clock rate by digital clock divider. Typically the GSM_DCM output clock no more than 52Mhz.

Note that PLL need some time to become stable after being powered up. The software shall take cares of the PLL lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL lock time is employed to deal with the problem.
For power management, the MCU software program may stop MCU Clock by setting the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode, and thus MCU return to the running mode.
AHB also can be stop by setting the Sleep Control Register. However the behavior of AHB in sleep mode is a little different from that of MCU. After entering Sleep Mode, it can be temporarily waken up by any "hreq"(bus request), and then goes back to sloop automatically after all "hreqs" de-assert. Any transactions can take place as usual in sleep mode, and it can save power while there is no transaction on it. However the penalty is losing a little system efficiency for switching on and off bus clock, but the impact is small

3.5 RFSYS of MT6253 (U101)

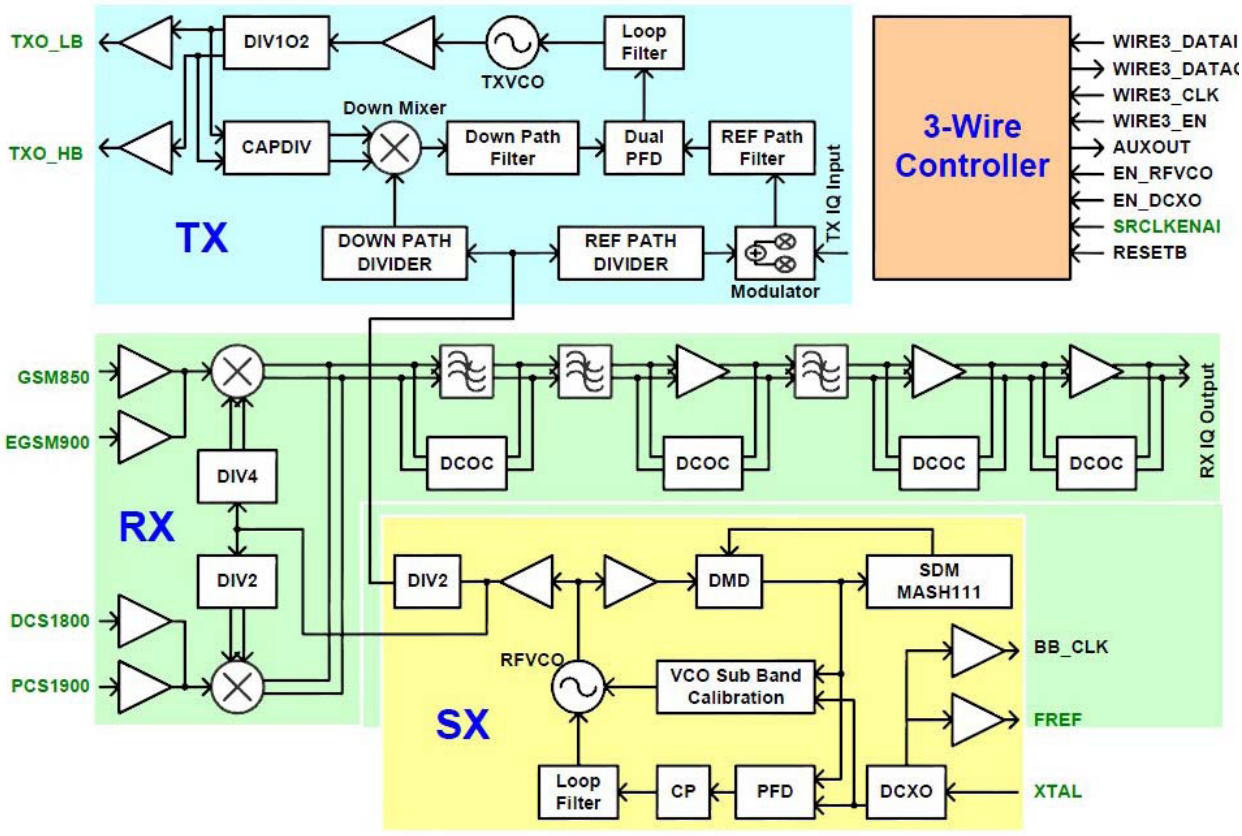


Figure. 3.5.1 Block DIAGRAM of RFSYS

3.5.1 GENERAL DESCRIPTION

RFSYS built in MT6253 SOC is a highly integrated RF transceiver for multi-band GMS and GPRS cellular systems. The features are listed as following.

- **Receiver**
  - Direct conversion architecture
  - Quad band differential input LNAs
  - Quadrature RF mixers
  - Fully integrated channel filter with f_{3dB}=150kHz
  - 95 dB gain with 60 dB gain control range

■ **Transmitter**
- Offset phase lock loop.
- IQ modulator.
- Integrated TX VCO.
- Integrated loop filter.

■ **Frequency Synthesizer**
- Programmable fractional-N synthesizer.
- Integrated wide range RFVCO.
- Integrated loop filter.
- Fast settling time suitable for multi-slot GPRS/EDGE applications.

■ **Digitally-Controlled Crystal Oscillator (DCXO)**
- One-pin 26 MHz crystal oscillator.
- On-chip programmable capacitor array for coarse tune.
- On-chip programmable capacitor array for fine tune.

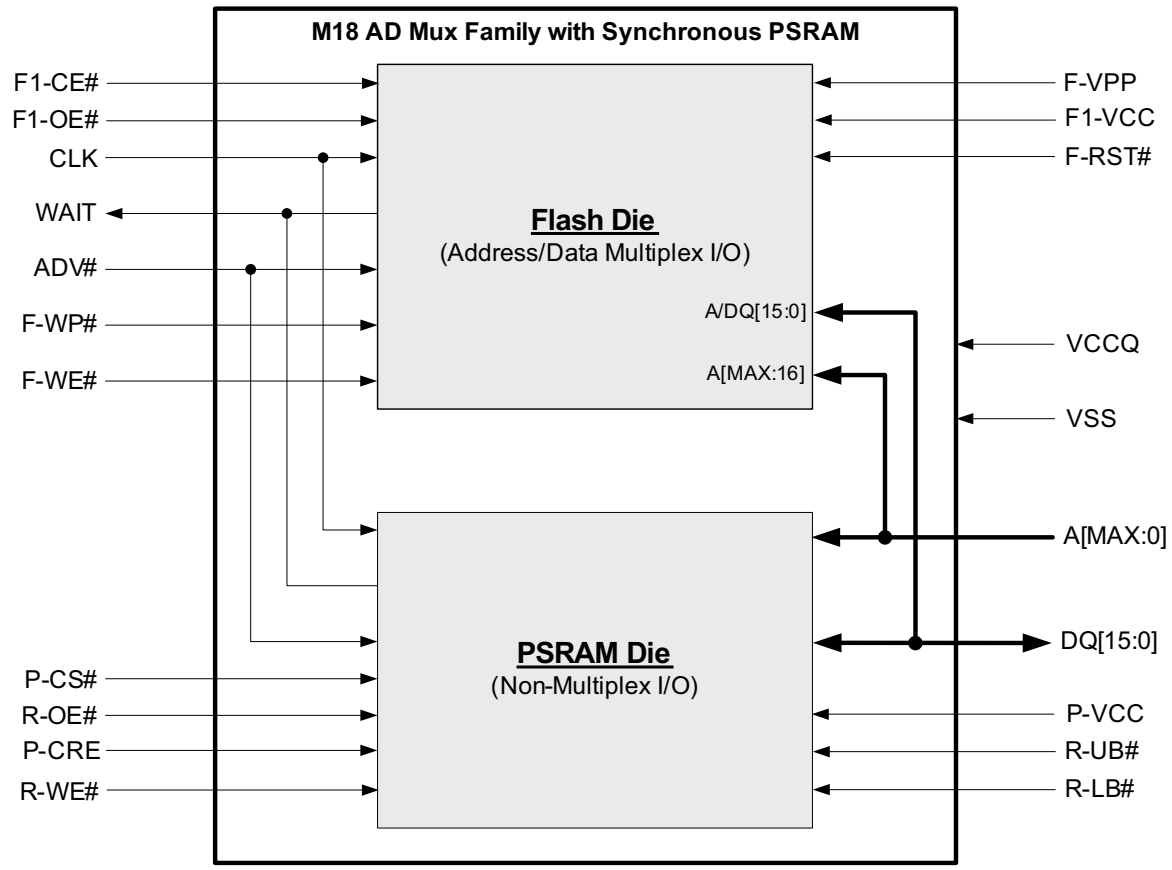
■ **RFSYS in a-QFN package**

3.6 MEMORY(PF38F5060M0Y3DK, U100)

3.6.1 Functional Description

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.
The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.
The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching (legacy-latching) on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table.

Sync PSRAM AD-Mux I/O Block Diagram.



Notes:

1. F2-OE# must be treated as an RFU, Howerver, to ensure future compatibility, F2-OE# can be tied to F1-OE# or left floated.
2. F2-VCC must be treated as an RFU, Howerver, to ensure future compatibility, F2-VCC can be tied to F1-VCC or left floated.
3. For full AD-Mux (NOR/PSRAM), PSRAM Address[15:0] are shared with NOR ADQ[15:0]; See Figure, " " on apge 27.
4. For full AD-Mux (NOR/PSRAM) all address/data are shared with NOR ADQ[15:0], Upper addresses [Max:16] should be connected to VSS.

Figure. 3.6.1 MEMORY BLOCK DIAGRAM

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	ADV# - and CLK-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	133	CLK-latching
	1024	108	ADV# - and CLK-latching
	1024	133	CLK-latching

Table 3_6_1 M18 Frequency combinations

In continuous-burst mode, a data Read can traverse partition boundaries.
Upon initial power-up or return from reset, the device defaults to asynchronous arrayread mode. Synchronous burst-mode reads are enabled by programming the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.
Designed for low-voltage applications, the device supports read operations with VCC at1.8 V, and erase and program operations with VPP at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when VPP is less than VPPLK.
A Status Register provides status and error conditions of erase and program operations
One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:
- Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.
- Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.
- Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiated by asserting the DPD pin.

3.6.2 Features

- **Device Architecture**
  - Flash Die Density: 128, 256, 512 Mbit, or 1Gbit.
  - PSRAM Die Density: 32Mbit to 512Mbit.
  - x16 Non-Mux, AD-Mux, or AAD-Mux I/O Interface Option.
  - Virtual Address Option.

- **Device Voltage**
  - Core: VCC = 1.8 V
  - I/O: VCCQ = 1.8 V

- **Device Packaging**
  - Ballout: x16C with 107 Active Balls, QUAD+ with 88 Active Balls, or LPCP 56-ball NOR/PSRAM AD-Mux.
  - Area: 6.2x7.7 mm to 11x13 mm.
  - Height: 1.0 mm to 1.4 mm.

- **PSRAM Performance**
  - 70 ns Initial Read Access.
  - 20 ns Asynchronous Page-Mode Read 133, 104, and 80Mhz with 5.5, 7, and 9ns Clock-to-Output Synchronous Burst-Mode Reads.
  - Configurable 4-, 8-, 16- and Continuous-Word Burst-Length Reads and Writes- Partial-Array and Temperature-Compensated Self Refresh- Programmable Output Impedance.

- **Quality and Reliability**
  - Extended Temperature –25 °C to +85 °C
  - Minimum 100K Flash Block Erase Cycles.
  - ETOX™ IX (Flash) and ETOX™ X (Flash)Technology on 128 Mbit, 256 Mbit, and 512Mbit M18 die; ETOX™ X (Flash) on 1 Gbit M18 die.

- **Flash Performance**
  - 96 ns Initial Read Access; 15 ns Asynchronous Page-Mode Read.
  - Up to 133 MHz with 5.5 ns Clock-to-Data Output Synchronous Burst-Mode Read.
  - Buffered Enhanced Factory and 1.8 V Low-Power Buffer Programming Modes:2 µs/Byte (Typ).
  - Deep Power-Down Mode: 2 µA (Typ).
  - Configurable Output Driver.

■ **Flash Architecture**
- Multi-Level Cell Technology.
- Hardware Read-While-Program/Erase.
- Symmetrically Blocked Array.
- Eight Partitions.
- Configurable 8-, 16-, or Continuous-Words Burst Length Reads.
- 2-Kbit One-Time Programmable User Protection Register Bits.
- Zero-Latency Block Locking.
- Automated Blank Check Mode.

■ **Flash Software**
- Numonyx™ FDI and Numonyx™ PSM.
- Common Flash Interface.
- Basic and Extended Flash Command Set.

3.7 BT & FM Module(MT6626, U401)

The connections between internal modules, as well as, external interfaces can be found in Figure 3.7.1
The Bluetooth transceiver section of MT6626 incorporates the complete receiving and transmitting Paths, including PLL, VCO, LNA, PA, modulator, and demodulator. The Bluetooth baseband signal processor incorporates hardware engines to perform frequency hopping, error correcting, whitening, encrypting, data packet assembling. The FM receiver section incorporates the complete receiving path with wide tuning range. The FM baseband signal processor incorporates the digital demodulator and audio processing function which provides superior audio quality as well as RDS/RBDS data service.

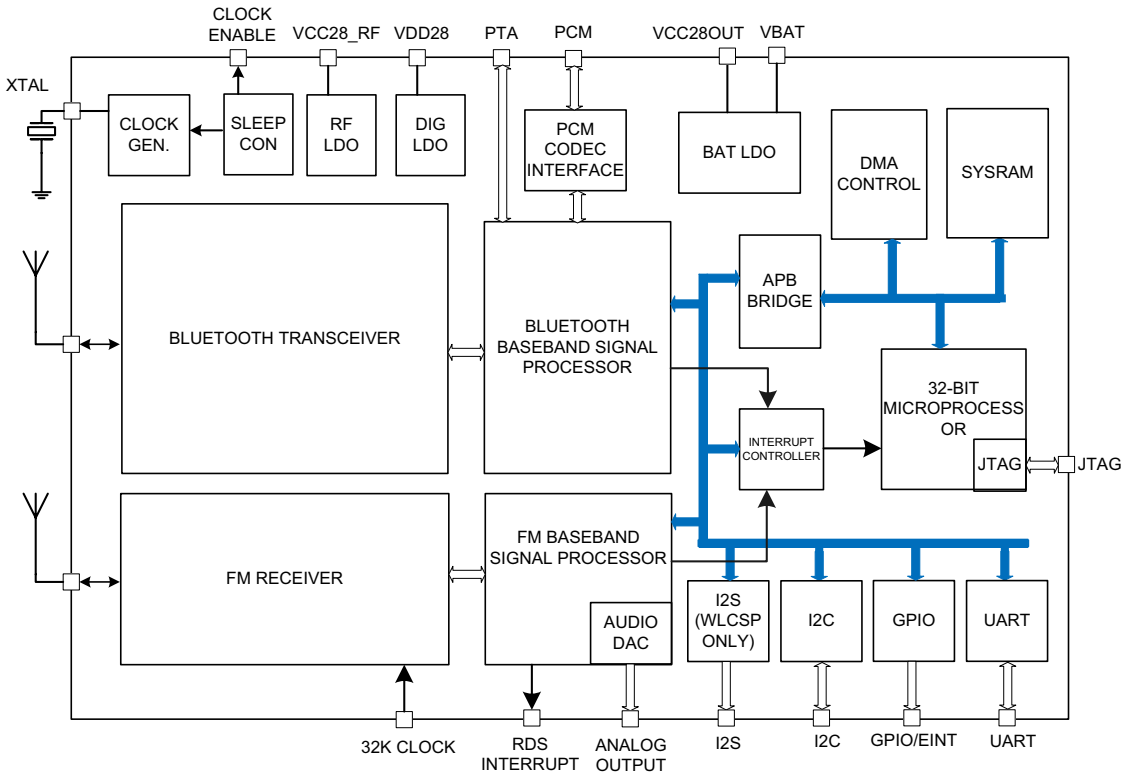


Figure 3.7.1. BT BLOCK DIAGRAM

3.7.1 General Description

MT6626 is a monolithic single chip that integrates Bluetooth v2.1+EDR and FM receiver. It can be incorporated in varieties of mobile platforms to provide Bluetooth connectivity and FM radio. MT6626 is available in QFN40 and WLCSP package. With a very small package size and require few external BOM components, a compact footprint can be designed for today's slim mobile device. Unparalleled performance of sensitivity and interference rejection featured, MT6626 also provides uncompromising low power performance. It also supports 10dBm transmit power with efficient power control, which provide the user with excellent link quality.

3.7.2 Feature

■ **BT Radio features**
- Fully compliant with Bluetooth specification 2.1 + EDR.
- Low out-of-band spurious emissions supports simultaneous operation with GPS, GSM/GPRS worldwide radio systems
- Integrated balun.
- Supports low power scan mode support.
- Fully integrated power amplifier provides 10dBm (class 1) output power.
- -95dBm sensitivity with excellent interference rejection performance.
- AGC dynamically adjusts receiver performance in changing environments.

■ **BT Baseband features**
- Support SCO and eSCO link with re-transmission.
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan Sniff mode support.
- AFH and PTA collaborative support for WLAN/BT coexistence.
- PCM interface and built-in transcoders for A-law, μ-law and linear voice with re-transmission support.
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening, and encryption.
- Channel quality driven data rate adaptation.
- Channel assessment for AFH.

■ **Platform features**
- 32-bit RISC microprocessor.
- Integrated LDO enables direct connection to battery.
- Wide range of frequency of crystal and external reference clock support.
- High speed UART supports up to 4Mbps baud rate.
- Built-in RAM and ROM with patch system.
- External LPO clock support for sleep mode and FM function. Supports standard HCI interface.
- Idle mode and sleep mode design enables ultra low power performance.

■ **FM features**
-76-108 MHz worldwide FM bands with 50KHz tuning step.
-RDS / RBDS radio data system support.
-Long/short antenna support.
-30ms seek time per channel, and 6sec search time for all channels.
-Superior stereo noise reduction.
-Supports 32.768KHz clock as reference clock.
-Soft mute volume control.
-Supports automatic short antenna calibration for different FM channels.
-60dB mono SINAD with 22.5KHz FM deviation.
-2dBuVemf sensitivity with superior interference rejection.
-20dBuVemf RDS sensitivity (dev: 2KHz).
-Support I2S digital interface (available in WLCSP package).

3.7.3 Functional Description

■ **Power Subsystem**

MT6626 contains several LV (low voltage, 2.8V to 1.5V) linear regulators to provide power supply for every power domain, including RF circuitry and digital core circuitry. Furthermore, it has built-in BAT linear regulator which allows the chip to connect directly to Li-Ion battery power supply. The supported battery voltage ranges from 3.2V to 4.3V.

The input pin LDO28EN is used by the host controller to turn on and off the BAT regulator. The host can control this pin to enable the whole MT6626 system. The enable voltage (VIH) of pin LDO28EN is 1.5V. Please be sure that the control signal meets this requirement in order for the system to operate correctly. The built-in LV linear regulators for RF circuitry are cap-less regulators. It provides high PSRR for achieving excellent RF performance. The power controls for these RF LDOs are maintained internally by digital controller for optimized power consumption.

The DIG (digital) LV regulator requires an external capacitor. When the 1.2V power is supplied from the regulator on VDD12 pins, an internal POR (Power-On Reset) will be generated to start the system. An external system reset to start the system is optional according to the application requirement.

■ **Clock generation**

There are two clock domains inside MT6626. One is the SYSTEM reference clock which is used for the Bluetooth and MCU system operations. The second is the LPO clock, which is a low-power 32.768KHz reference clock used for FM system and also maintaining Bluetooth link during sleep mode operations. The use of the LPO clock for FM system allows the entire MT6626 to be operating in the lowest possible power consumption mode when the rest of the system is under sleep state.

MT6626 has two options for the SYSTEM clock source input. It can either be a one-pin crystal input, or it can come from external clock source. MT6626 supports most widely used clock frequencies in the mobile handset platform. They include 13, 16, 19.2, 26, and 32MHz.

To save system BOM cost, the SYSTEM clock can be shared with the clocks available on the mobile handset platform. For example, the reference clock used for mobile base-band chipset can also be used as the MT6626 source clock. In this configuration, an output pin SRCLKENA from MT6626 is used as the enable signal for the external clock source. The generation of the signal is coupled to the internal sleep mode control function. The input frequencies can be selected by GPIO trapping or detected automatically based on the availability of externally supplied 32.768KHz clock.

The LPO clock can come from the host chip in both QFN40 and WLCSP package, or an external oscillator for WLCSP only.

■ **Chip power management**

MT6626 is designed such that Bluetooth and FM functions can be operated concurrently and independently without interference. With sophisticated built-in state control and advanced power management, the operating mode can be changed seamlessly while achieving minimum power consumption.

MT6626's operating modes can be categorized into 6 major modes

- Chip power off mode.
- Power-on Init mode.
- Bluetooth standalone operation mode.
- FM standalone operation mode.
- Bluetooth + FM concurrent operations mode.
- System deep sleep mode.

■ **MCU Subsystem**

The MCU (Micro-Controller Unit) subsystem contains the 32-bit RISC microprocessor, internal memory and the ROM patch function. It also contains the UART interface controller and the power/clock management function.

■ **Bluetooth Subsystem**

The Bluetooth subsystem contains the Bluetooth baseband subsystem and the Bluetooth RF subsystem.
The Bluetooth baseband subsystem contains a baseband processor which supports timing control, bit-stream processing, encryption, frequency hopping, and modulation/demodulation. It also contains the audio codec, Wi-Fi coexistence interface controller, and a sleep mode controller.
The Bluetooth RF subsystem contains a fully integrated transceiver. For TX path, the baseband transmit data is digitally modulated in the baseband processor, then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter, and the power amplifier. The power amplifier is capable of transmitting 10dBm power for class-1.5 operation.
For RX path, MT6626 is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which could support different clock frequencies as the reference clock as described in section 4.2. The mixer output is then converted to digital signal, down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.
MT6626 features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

■ **FM Subsystem**

MT6626's FM radio subsystem provides a completely integrated FM RX receiver supporting 76-108 MHz FM bands with 50KHz tuning step. It also performs fast channel seek/scan algorithm to validate 200 carrier frequencies in 6 seconds. In addition to receive FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.
In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize RX system performance in all range of signal quality by reference of a very sophisticated channel quality indicator (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.
The FM subsystem requires only the availability of the 32.768KHz clock input, and can be operated completed independently from the Bluetooth subsystem. Therefore, allowing for full simultaneous operation and coexistence with the Bluetooth subsystem while maintaining the most power-efficient consumption under different operating states.
The FM subsystem supports high performance stereo analog line out. In WLCSP package, it also supports digital audio out.

3.8 SIM Card Interface

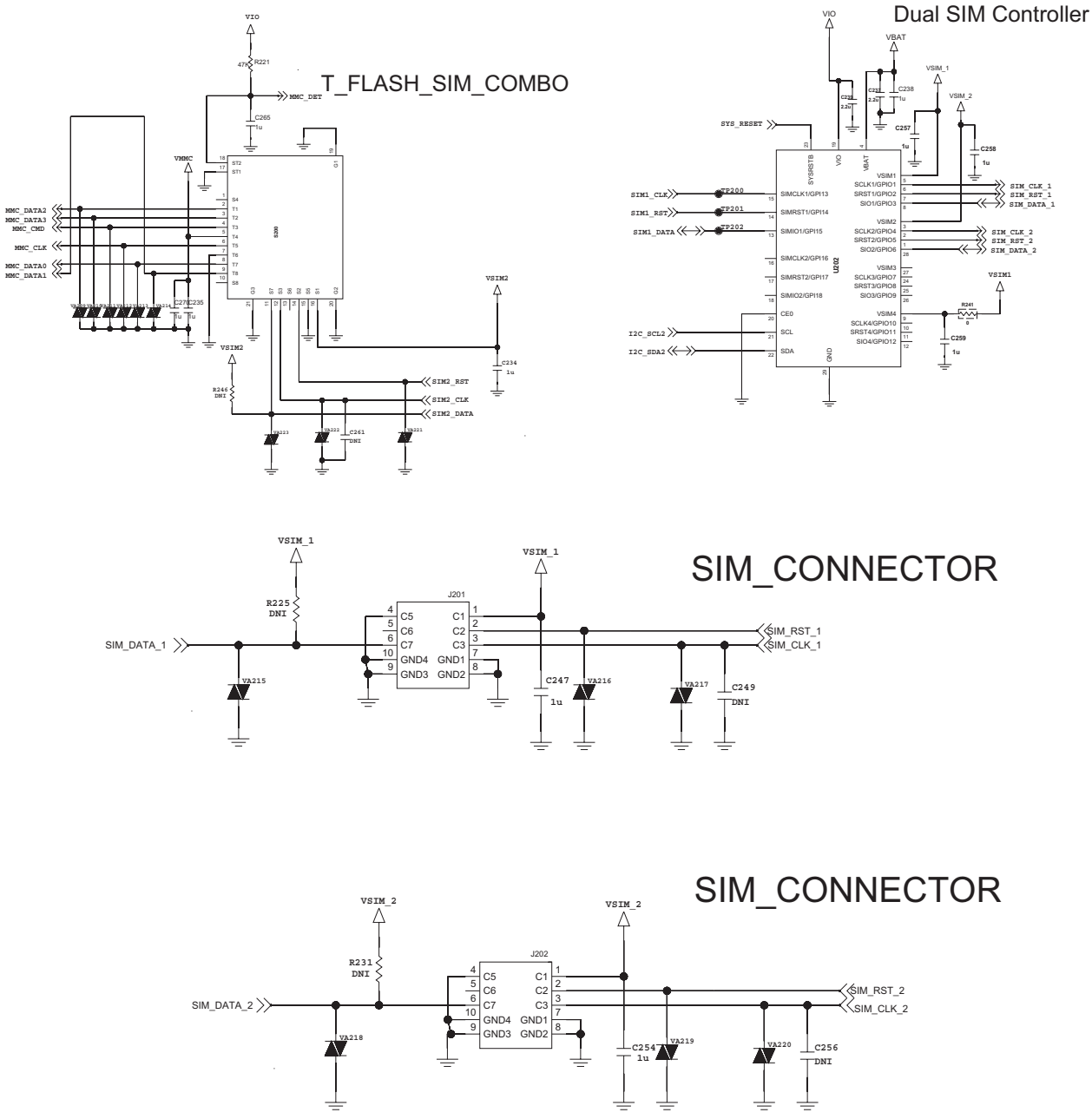


Figure 3.8.1 SIM Connector Circuit Diagram

The Main Base Band Processor(MT6253) contains two dedicated smart card interfaces to allow the MCU to access the two SIM cards. Each interface can operator via 5 terminals. As shown is the Figure 3.8.2, SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA are for one SIM interface, while SIM2VEE, SIM2SEL, SIM2RST, SIM2CLK and SIM2DATA are for the other one. The functions of the two SIM interfaces are identical; therefore, only first SIM interface will be described in this document. The VSIM is used to control the external voltage supply to the SIM card and SIM SEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose.

A290 is using U202 as SIM controller to be able to use triple SIM.

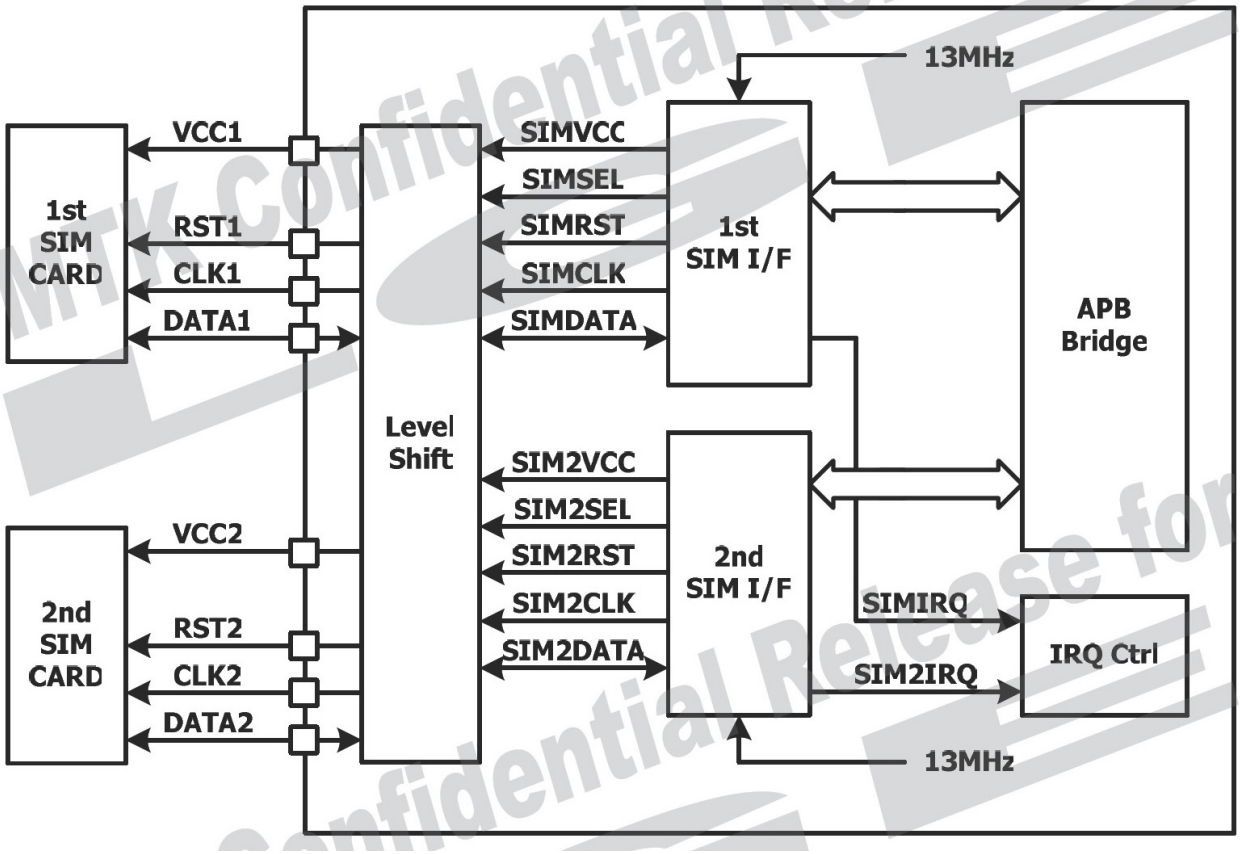


Figure 3.8.2 SIM Interface block diagram

3.8.1 Dual SIM controller(MT6306, U202)

■ **General Description**

The MT6306 is a SIM card / GPIO control chip optimized for GSM handsets, especially those based on the MediaTek MT62xx system solution. It supports up to four SIM interfaces or 12 GPIOs plus six GPIs. Each SIM interface can be individually programmed as GPIOs. The SIM interface supports both 1.8V and 3V SIM cards. An I2C interface is used to control SIM channel individually.
The MT6306 is available in 28-pin 4mm x 4mm QFN package. The operating temperature range is from -25°C to +85°C.

■ **Features**

Control and communication through an I2C interface with baseband processor.Independent 1.8V/3V VCC control for each SIM cardPower management and control for quad SIM cardsIndependent clock stop mode (at high or low level) for each SIM cardProgrammable SIM interface pins (can be SIM interface pins or GPIO pins)Compatible with MediaTek baseband processor chips, MT6252, MT6253, MT6235, MT6236, etc.28-Pin 4mm x 4mm QFN Package.

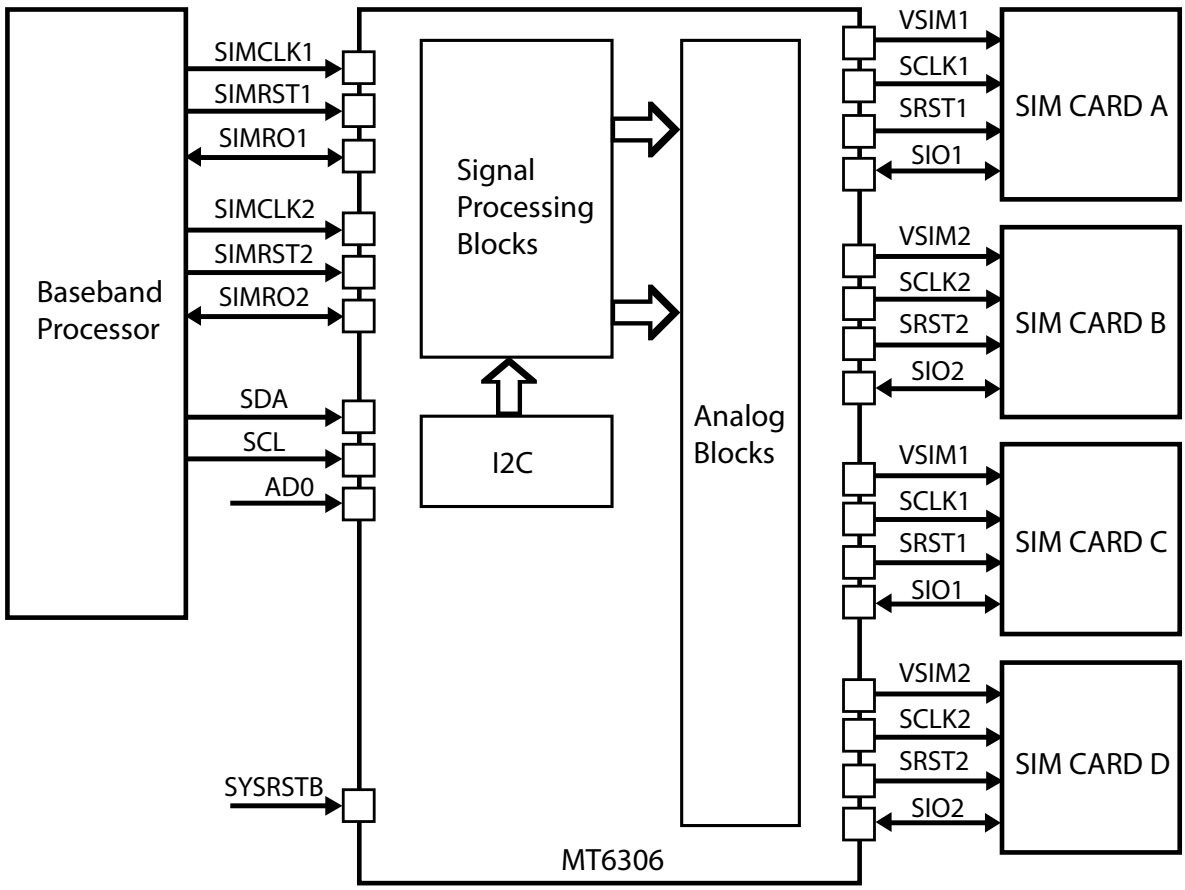


Figure 3.8.3 SIM Controller block diagram

3.9 Micro-SD Card Interface

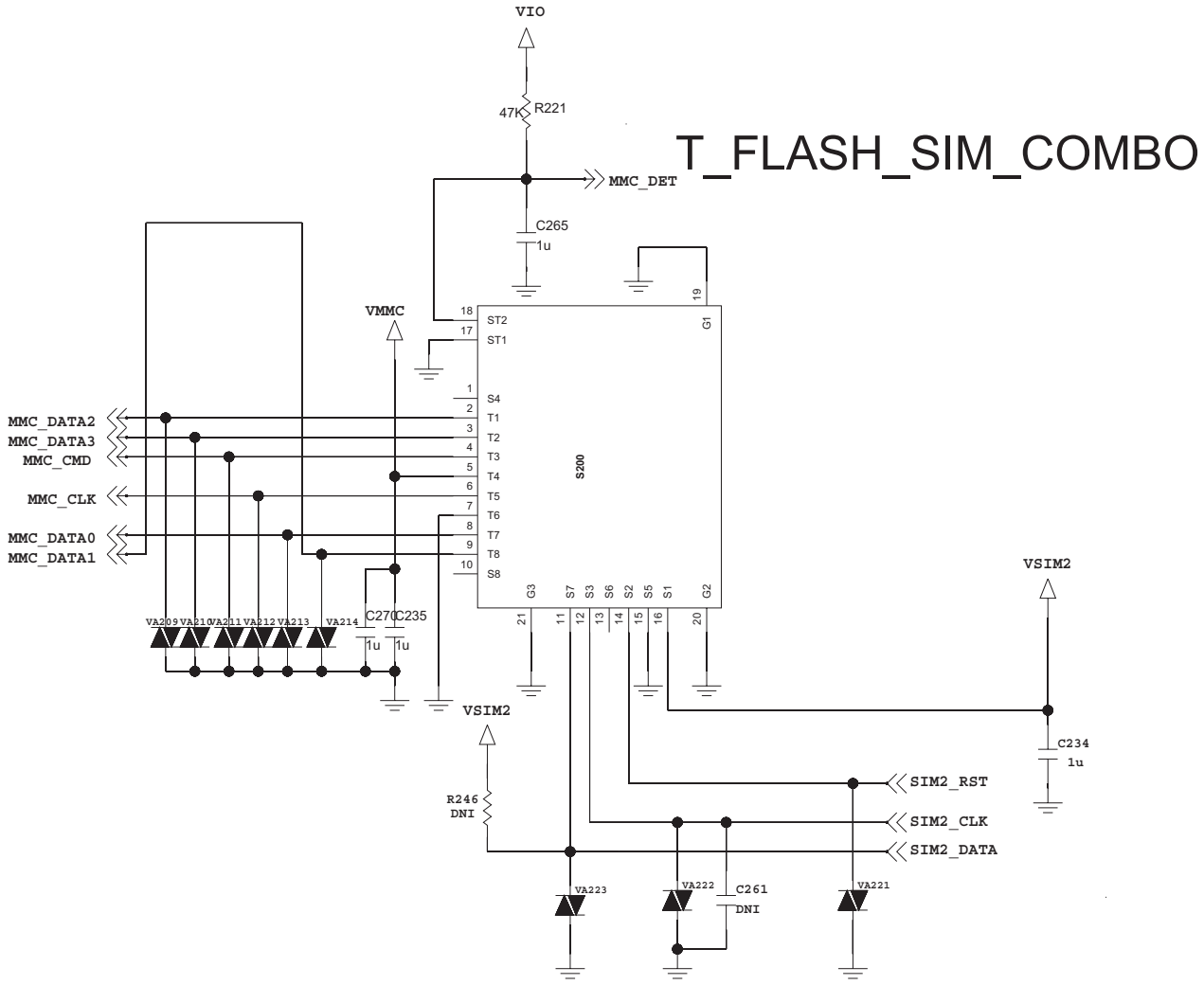


Figure 3.9.1 Micro-SD Card Interface

The controller fully supports the Memory Stick bus protocol as defined in Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) and the SD Memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 as well as the Multi Media Card(MMC) bus protocol as defined in MMC system specification version 4.1. Since SD memory Card bus protocol is backward compatible to MMC bus protocol, the controller is capable of working well as the host on MMC bus under control of proper firmware. Furthermore, the controller also support SDIO card specification version 1.0 partially. However, the controller can only be configured as either the host controller.

3.9.1 Pin Assignment

Since the controller can only be configured as either the host of Memory Stick or the host of SD/MMC Memory Card at one time, pins for Memory Stick and SD/MMC Memory Card are shared in order to save pin counts. The following lists pins required for Memory Stick and SD/MMD Memory Card. Figure 3.9.2 shows how they are shared. In Table 3.9.1, all I/O pads have embedded both pull up and pull down resistor because they are shared by both the Memory Stick and SD/MMC Memory Card. Pins 2,4,5,8 are only useful for SD/MMC Memory Card. Pull down resistor for these pins can be used for power saving. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistor are required on the system board. The pin VDDPD is used for power saving. Power for Memory Stick or SD/MMC Memory Card can be shut down by programming the corresponding control register. The pin WP(Write Protection) is only valid when the controller is configured for SD/MMC Memory Card. It is used to detect the status of Write Protection Switch on SD/MMC Memory Card.

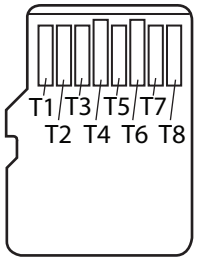
NO.	Name	Type	MMC	SD	MS	MSPRO	Description
1	SD_CLK	0	CLK	CLK	SCLK	SCLK	Clock
2	SD_DAT3	I/0/PP		CD/DAT3		DAT3	Data Line [Bit 3]
3	SD_DAT0	I/0/PP	DAT0	DAT0	SDI0	DAT0	Data Line [Bit 0]
4	SD_DAT1	I/0/PP		DAT1		DAT1	Data Line [Bit 1]
5	SD_DAT2	I/0/PP		DAT2		DAT2	Data Line [Bit 2]
6	SD_CMD	I/0/PP	CMD	CMD	BS	BS	Command Or Bus State
7	SD_PWRON	0					VDD ON/OFF
8	SD_WP	I					Write Protection Switch in SD
9	SD_INS	I	VSS2	VSS2	INS	INS	Card Detection

Table 3.9.1 Sharing of pins for Memory Stick and SD/MMC Memory Card controller

[microSD CARD PIN_MAP]

PIN NUMBER	DESCRIPTION
T1	DAT2
T2	CD/DAT3[2]
T3	CMD
T4	V_{DD}
T5	CLK
T6	Vss[2]
T7	DAT0
T8	DAT1

microSD CARD



3.9.2 Card Detection

For SD/MMC Memory Card, detection of card insertion/removal by hardware is also supported. Because a pull down resistor with about 470 KΩ resistance which is impractical to embed in an I/O pad is needed on the signal CD/DAT3, and it has to be capable of being connected or disconnected dynamically onto the signal CD during initialization period, an additional I/O pad is needed to switch on/off the pull down resistor on the system board. The scenario of card detection for SD/MMC Memory Card is shown in Figure 3.9.2. Before SD/MMD Memory Card is inserted or powered on, SW1 and SW2 shall be opened for card detection of the host side. Meanwhile, pull down resistor RCD on system board shall attach onto the signal CD/DAT3 by the output signal RCDEN. In addition, SW3 on the card is default to be closed. Upon insertion of SD/MMC Memory Card the signal CD/DAT3 will have a transition from low to high. If SD/MMC Memory Card is removed then the signal CD/DAT3 will return to logic low. After the card identification process, pull down resistor RCD on system board shall disconnect with the signal CD/DAT3 and SW3 on the card shall be opened for normal operation. Since the scheme above needs a mechanical switch such as a relay on system board, it is not ideal enough. Thus, a dedicated pin "INS" is used to perform card insertion and removal for SD/MMC. The pin "INS" will connect to the pin "VSS2" of a SD/MMC connector.

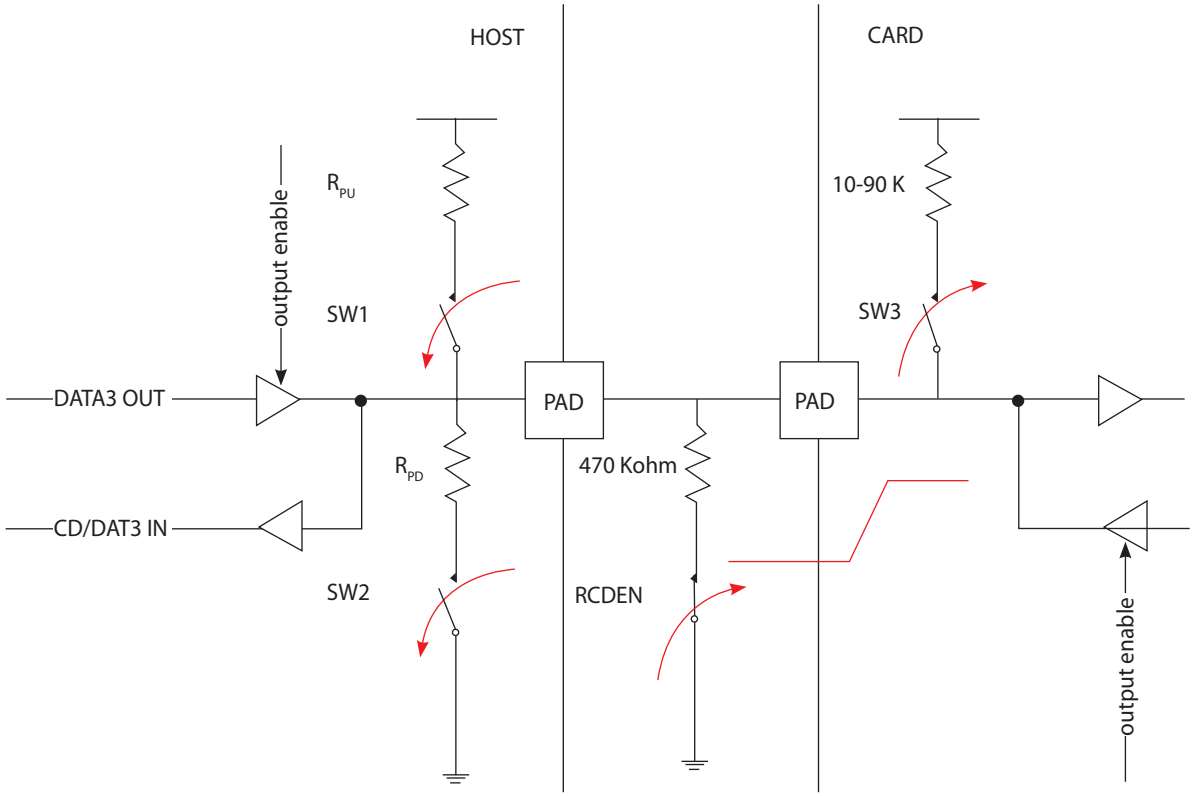


Figure 3.9.2 Card Detection for SD/MMC Memory Card

3.10 LCD Interface

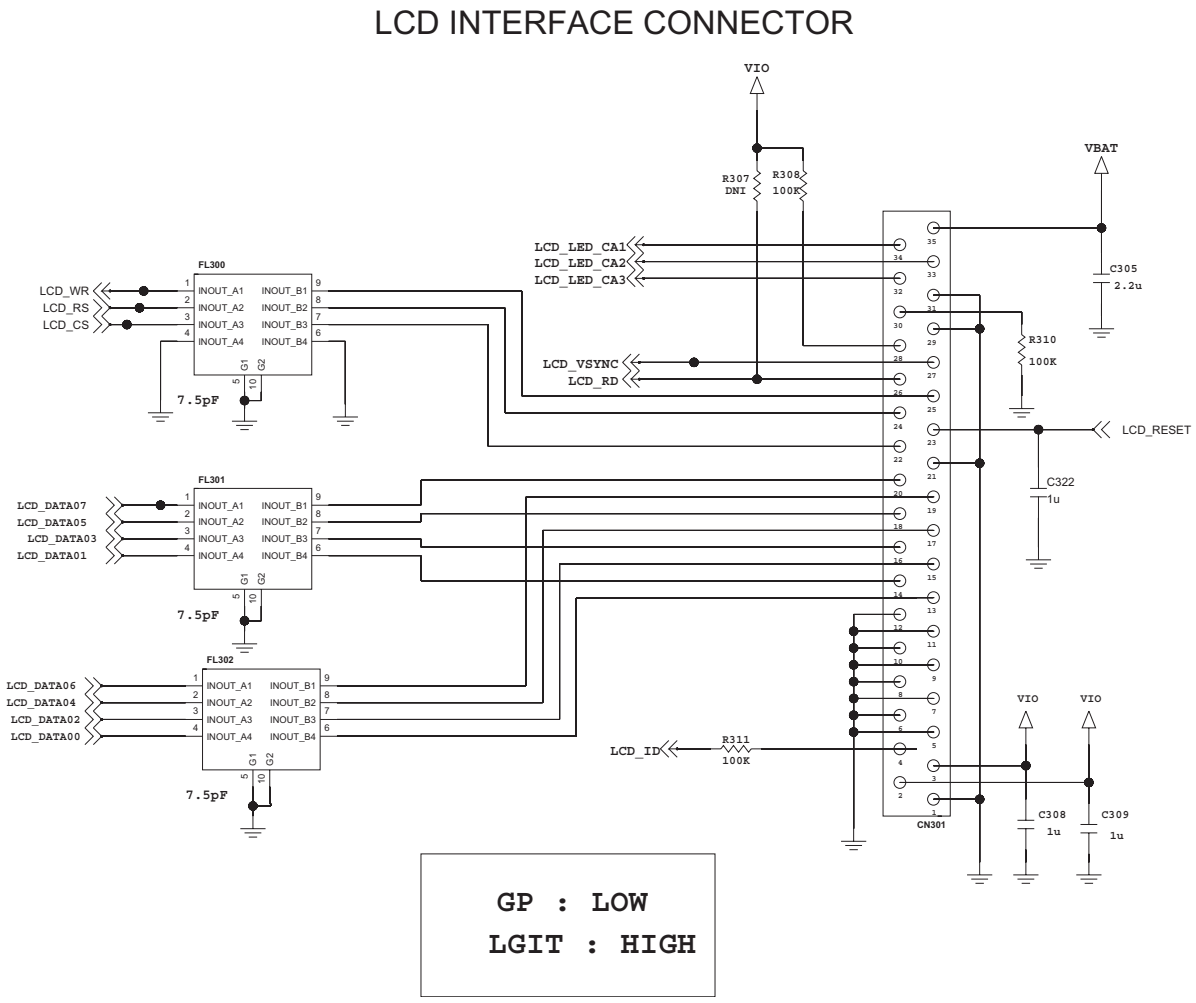


Figure 3.10.1 LCD Interface

ILI9225 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87120 bytes RAM for graphic data of 176RGBx220 dots, and power supply circuit.

ILI9225 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD.

The ILI9225 also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the ILI9225 an ideal LCD driver for medium or small size portable products such as digital cellular phones or small PDA, where long battery life is a major concern.

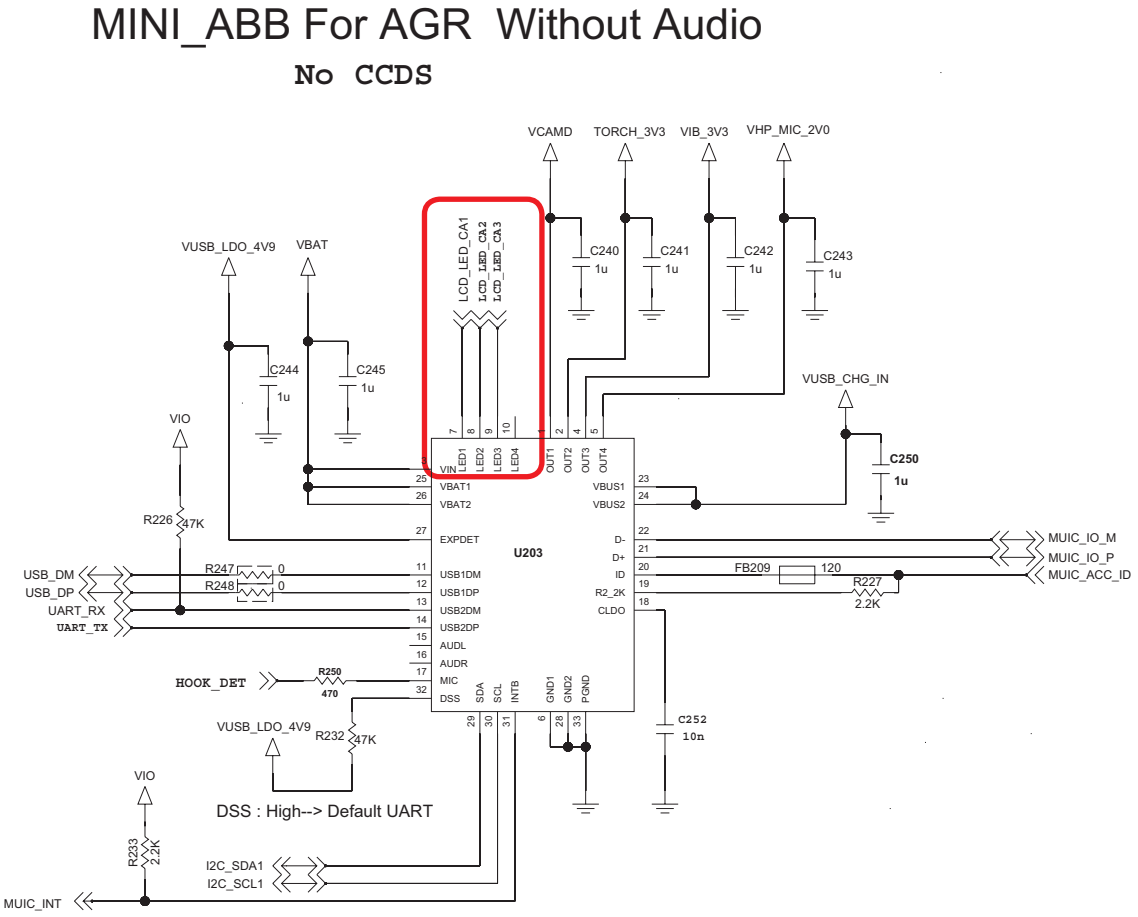


Figure 3.10.2 MINI ABB for LCD Backlight Source

The SNB1058A0RSMR is an integrated solution for backlighting(current sink type).

Address : 0x0D LED Conreol (LED _SET)

Data (7:0)	Entity	Access	Function
1001 1111			Default setting
000x xxxx ~ 111x xxxx	LED_ISET[2:0]	R/W	000 : 2.5mA 001 : 5mA 010 : 10mA 011 : 15mA 100 : 20mA 101 : 25mA 110 : 30mA 111 : 30mA

3.11 Battery Charger Interface / MUIC

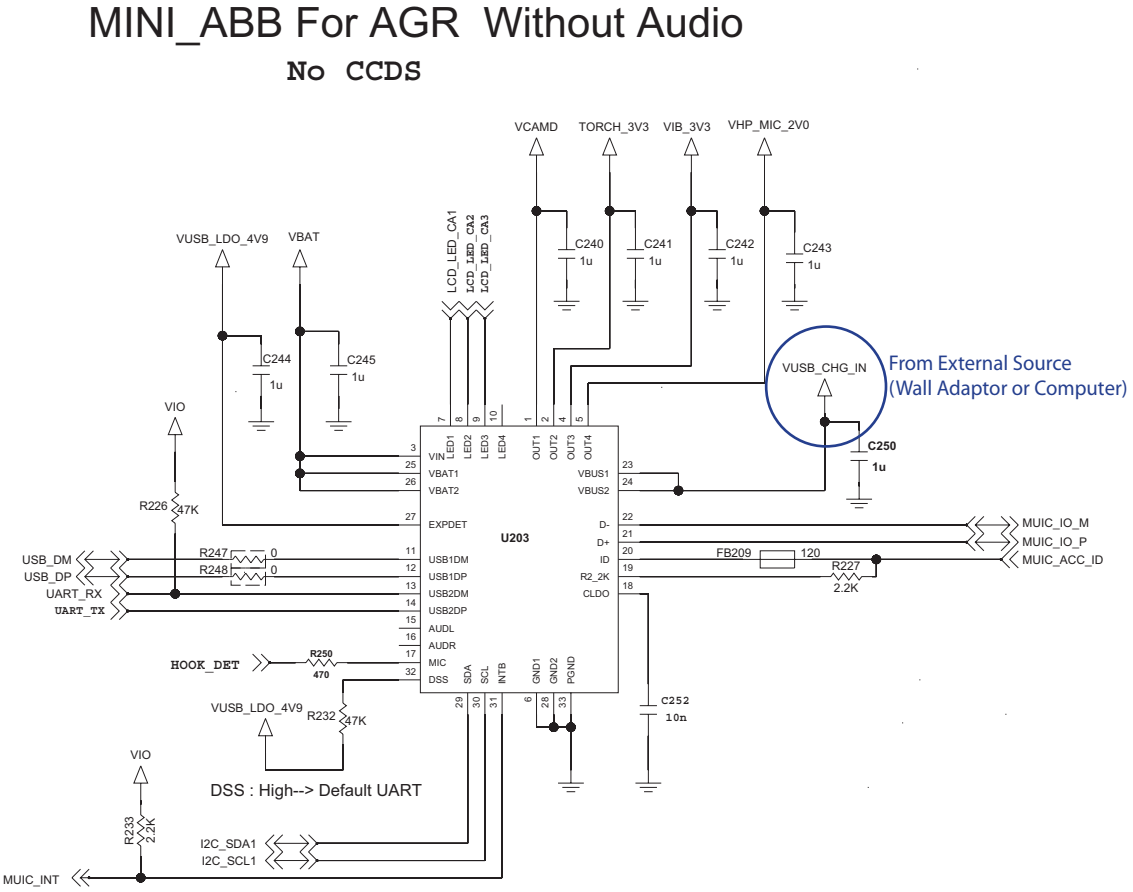


Figure 3.11.1 BATTERY CHARGER BLOCK

The McKinney is designed to interface the cell phone USB, and audio chips with external peripherals via a micro-USB connector. The switch features impedance detection for identification of various accessories that are attached through DP and DM of the micro-USB port. When an accessory is plugged into the micro-USB port, the switch uses a detection mechanism to identify the accessory (see the State Machine for details). It will then switch to the appropriate channel—data, audio, or USB.

The McKinney has an I2C interface for communication with the cell phone baseband or applicationsprocessor. An interrupt is generated when anything plugged into the micro-USB is detected. Another interrupt is generated when the device is unplugged.

The McKinney also provides a linear charger up to 1.1A charging current, 4 channel LED current drive(max 150mA) and 4 linear regulators.

If VBUS is higher than 4.0V and lower than 7.5V (programmable 6.0V ~ 7.5V through I2C) and 250mV higher than VBAT then charger starts charging automatically. If VBAT is below 2.5V, McKinney starts pre-charge mode with 80mA charging current until VBAT reaches 2.5V and switch to fast charge mode with soft start. When battery voltage approaches programmed regulation voltage(4.2V default), CV charging mode starts with programmed regulation voltage. At CV mode, if charging current reaches programmed full charge current, the device generates interrupt to notice charging full condition and start charge off timer. If charger off timer is disabled, charger stays at CV mode until stopped by system control.

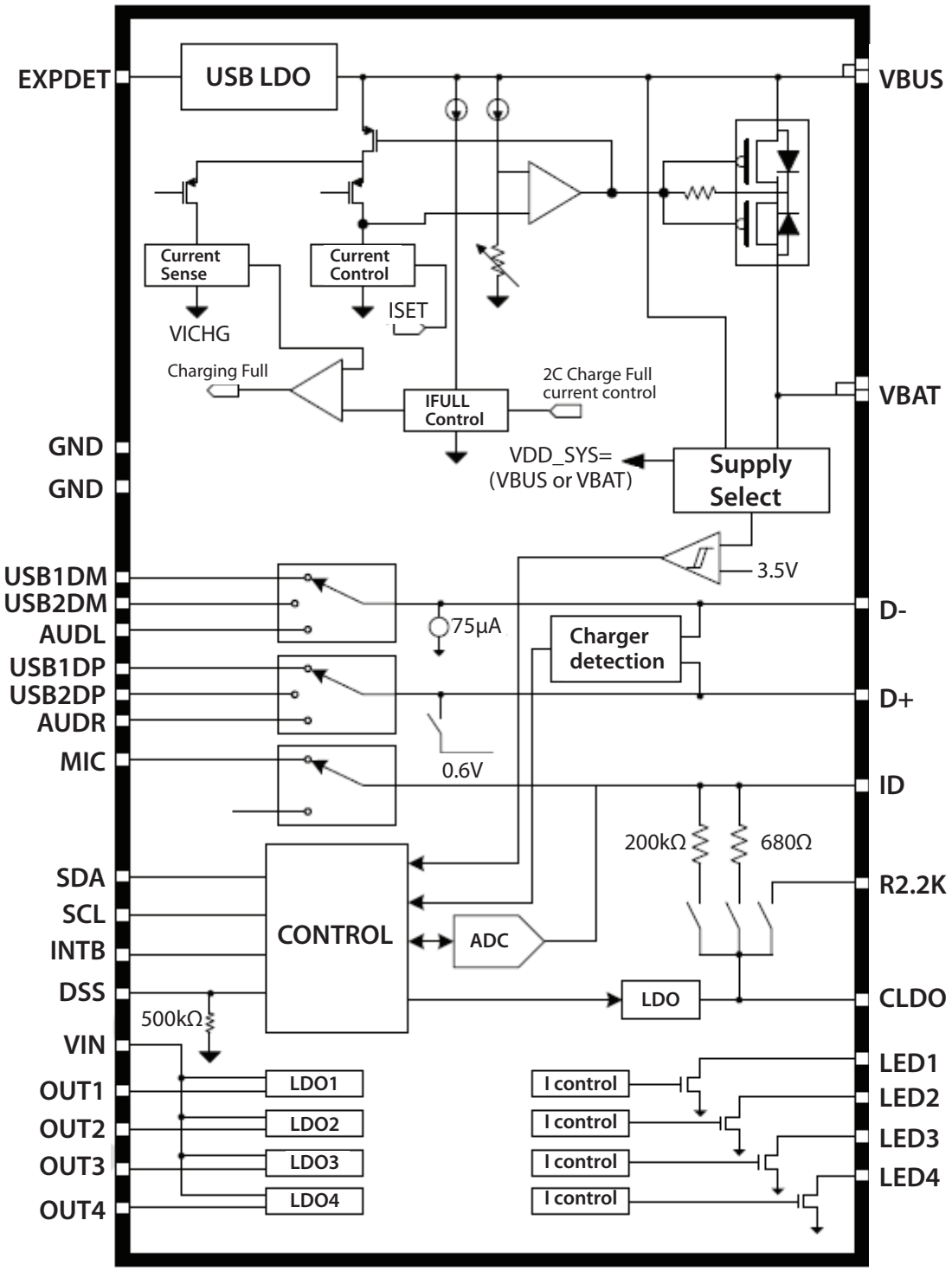


Figure 3.11.2 MINI ABB BLOCK DIAGRAM

3.12 Keypad Interface

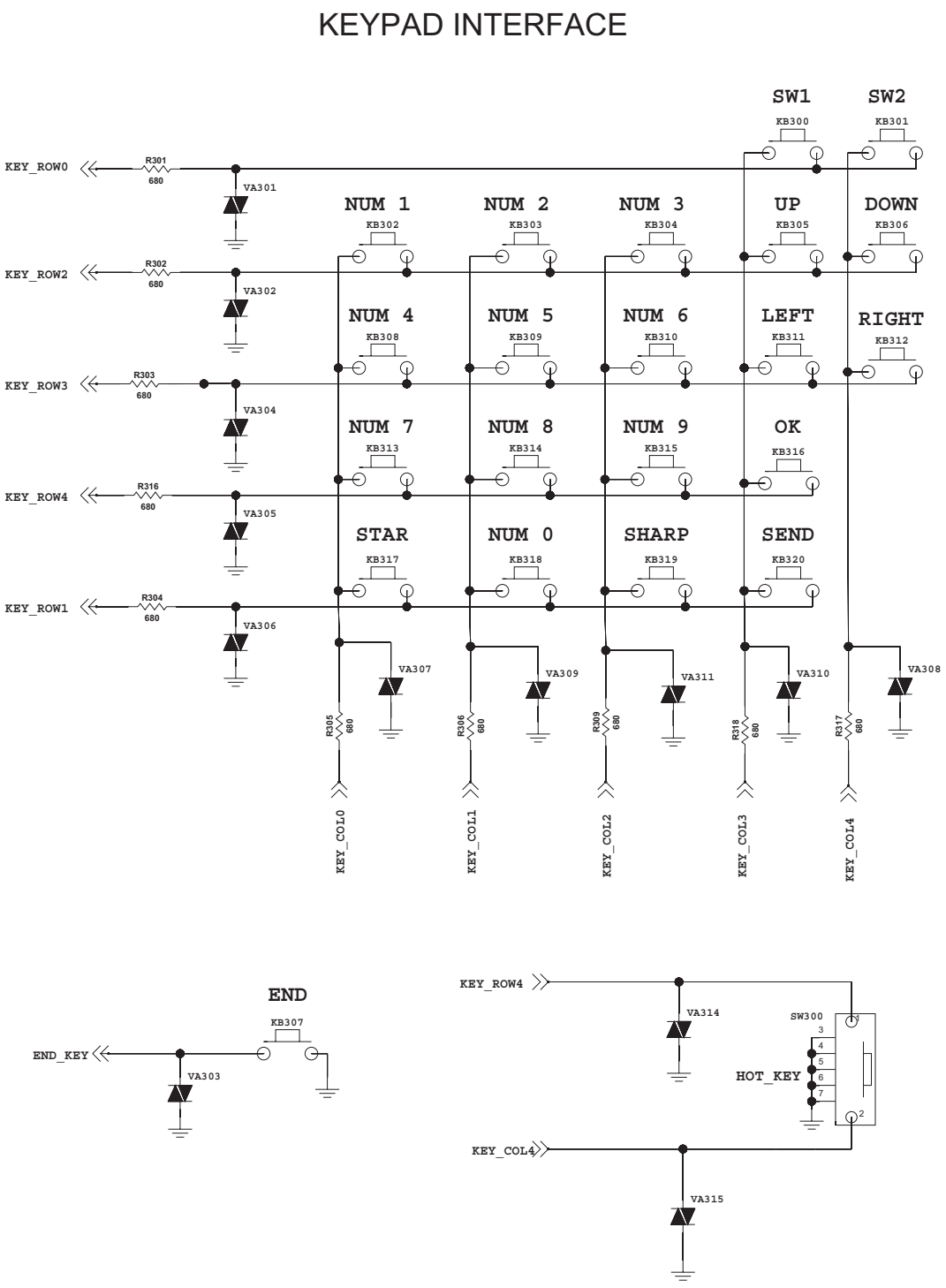


Figure 3.12.1 MAIN KEY STRUCTURE

The keypad can be divided into two parts: one is the keypad interface including 7 columns and 6 rows(A290 is using 5columns and 5rows) with one dedicated power-key, as shown in Figure 3.12.2; the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 6 x 7 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in KP_MEM1, KP_MEM2, KP_MEM3, and KP_MEM4 registers. To ensure that the key pressed information is not missed, the status register in keypad is not read-cleared by APB read command. The status register can only be changed by the key-pressed detection FSM.

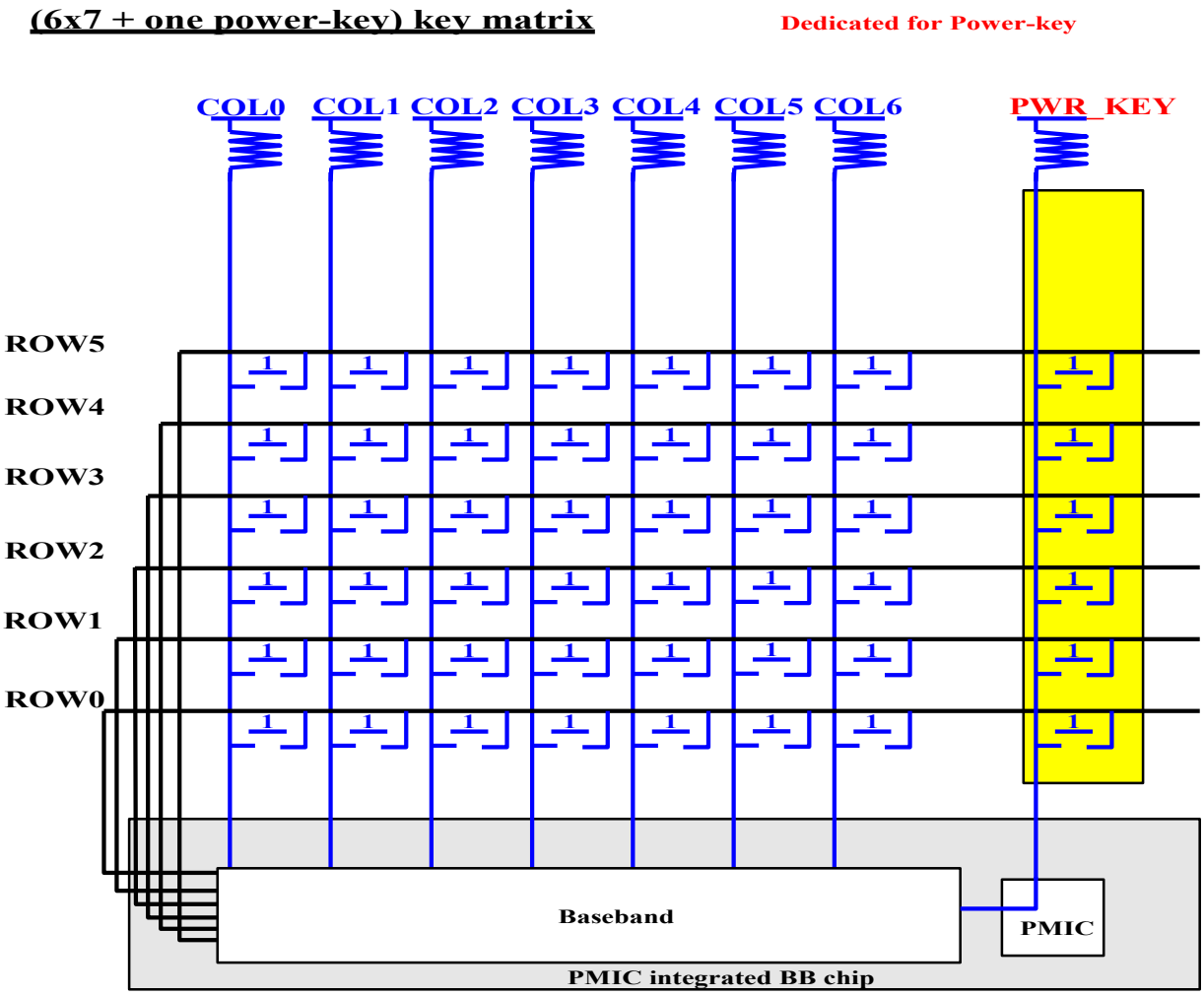


Figure 3.12.2 6x7 matrix with one power-key

This keypad can detect one or two key-pressed simultaneously with any combination. Figure 3.12.3 shows one key pressed condition. Figure 3.12.4(a) and Figure 3.12.4(b) illustrate two keys pressed cases. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

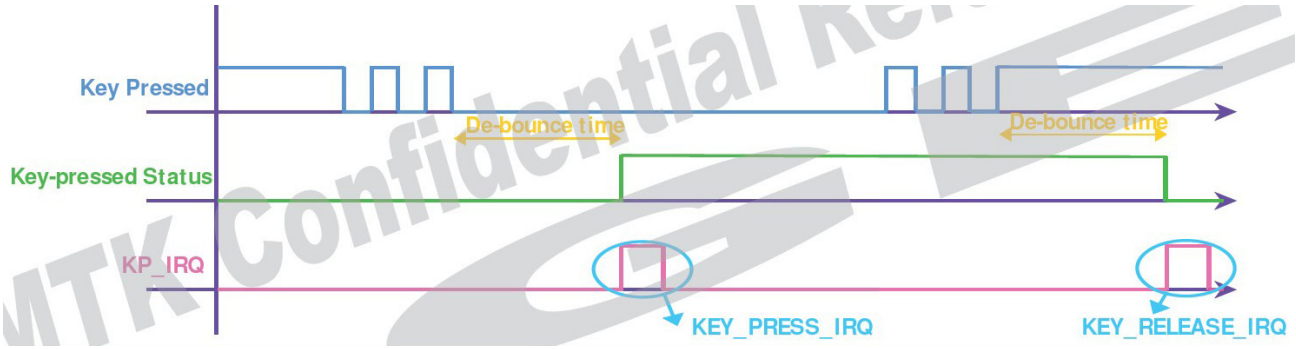


Figure 3.12.3 One key pressed with de-bounce mechanism denoted

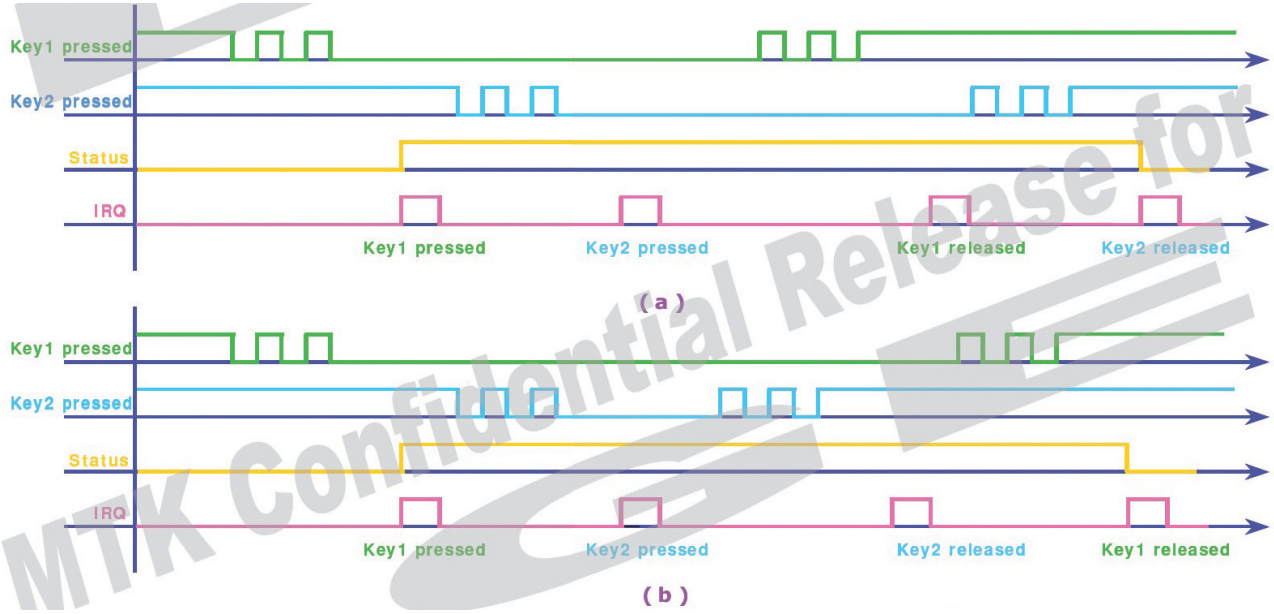


Figure 3.12.4 Two keys pressed, case 1 (b) Two keys pressed, case 2

3.13 Audio Front-End

3.13.1 General Description

The audio front-end essentially consists of voice and audio data paths. Figure 3.13.1 shows the block diagram of the audio front-end. All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset.

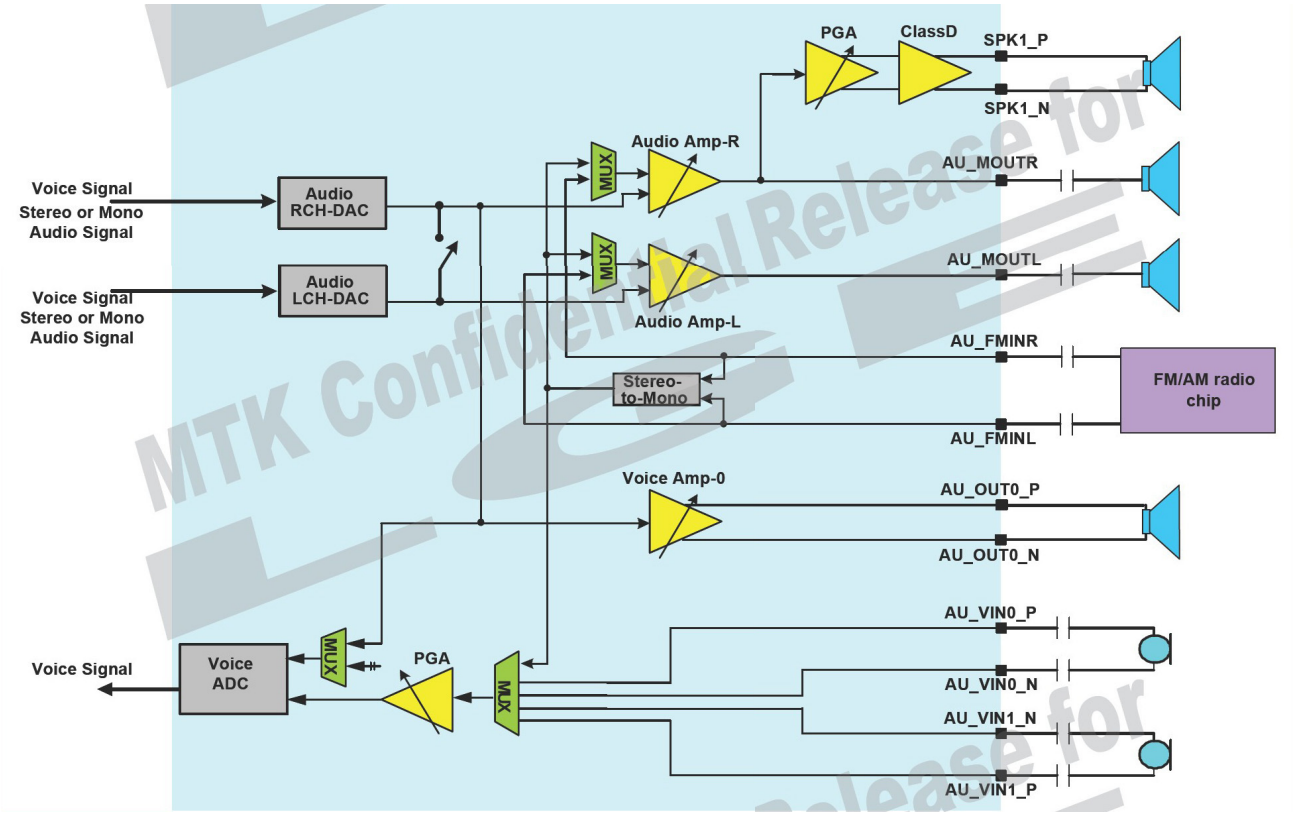


Figure 3.13.1 Block diagram of audio front end

Figure 3.13.2 shows the digital circuits block diagram of the audio front-end. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port (DAP) block interfaces with the DSP for control and data communications. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the System Simulator for FTA or external Bluetooth modules.

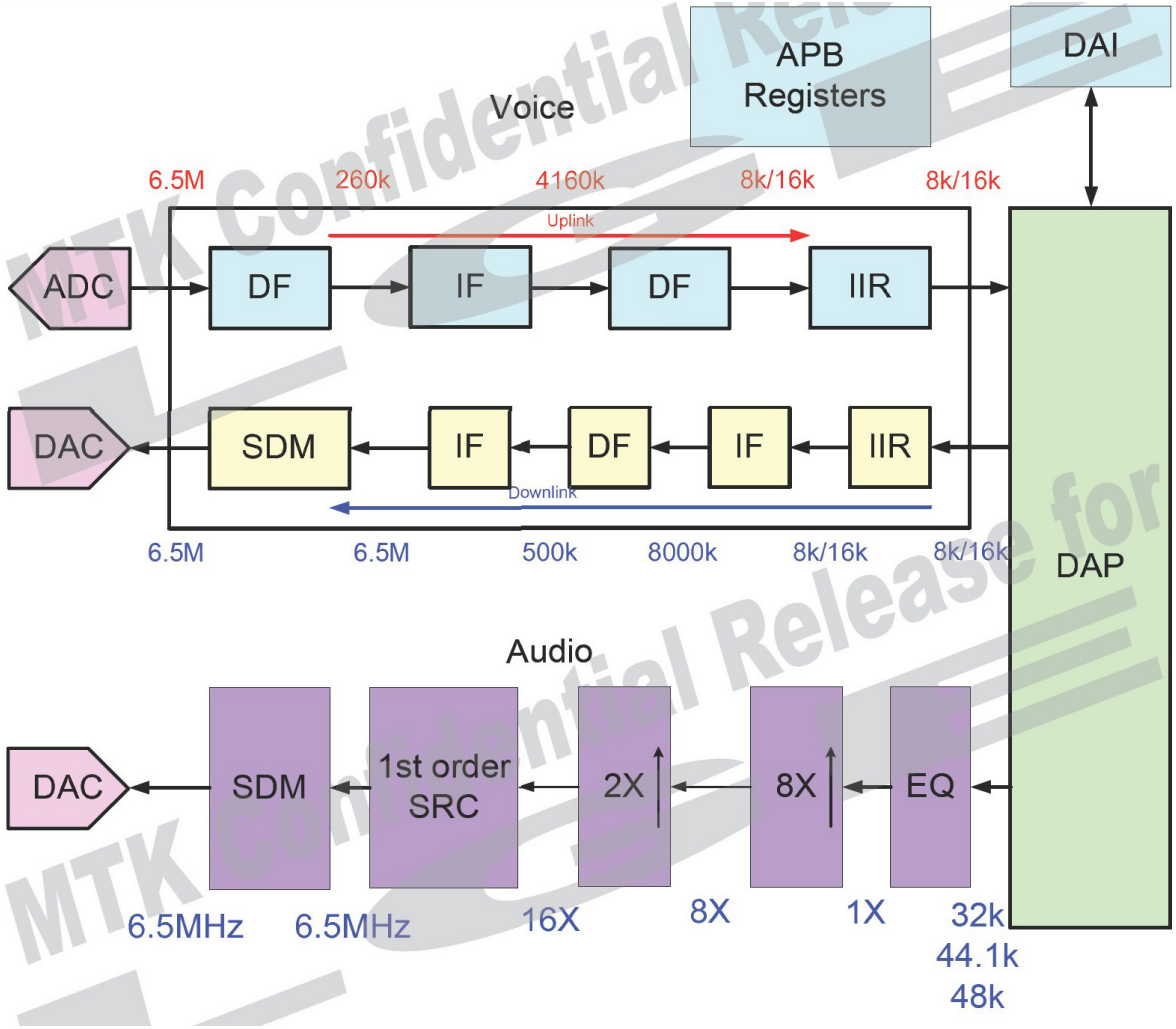


Figure 3.13.2 Block diagram of digital circuit of audio front end

To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256 kHz while the frame sync is 8 kHz. Both long sync and short sync interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8 kHz sampling rate voice signal. Figure 3.13.3 shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is rising and is latched when the clock is falling.

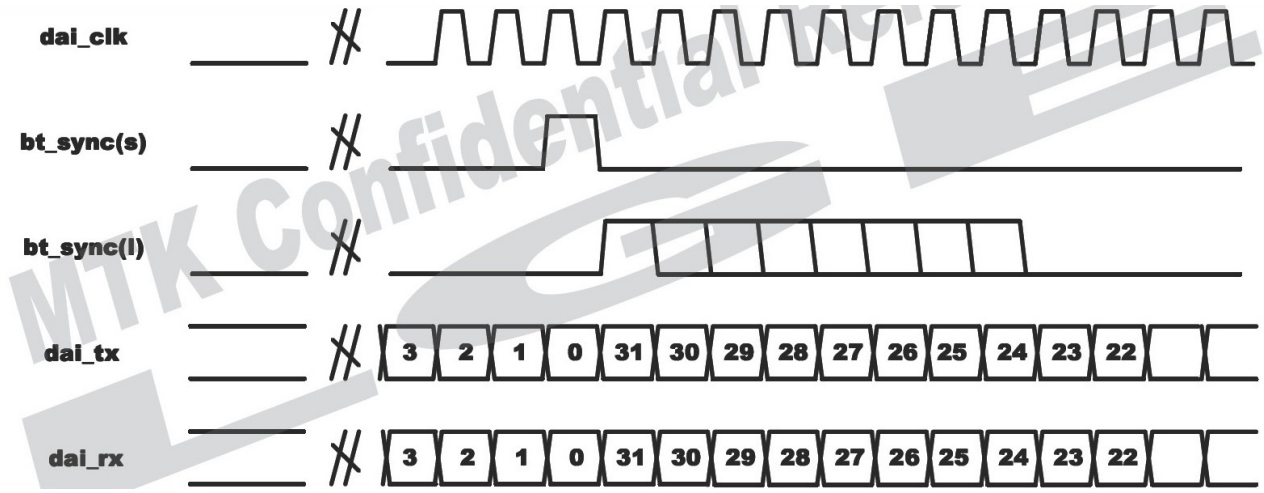


Figure 3.13.3 Timing diagram of Bluetooth application

I2S/EIAJ interface is designed to transmit high quality audio data. Figure 3.13.4 and Figure 3.13.5 illustrate the timing diagram of the two types of interfaces. I2S/EIAJ can support 32 kHz, 44.1 kHz, and 48 kHz sampling rate audio signals. The clock frequency of I2S/EIAJ can be 32×(sampling frequency), or 64×(sampling frequency). For example, to transmit a 44.1 kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112 MHz or 64 × 44.1 kHz = 2.8224 MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. Audio data can easily be sent to the external DAC through the I2S/EIAJ interface. In this document, the I2S/EIAJ interface is referred to as EDI (External DAC Interface).

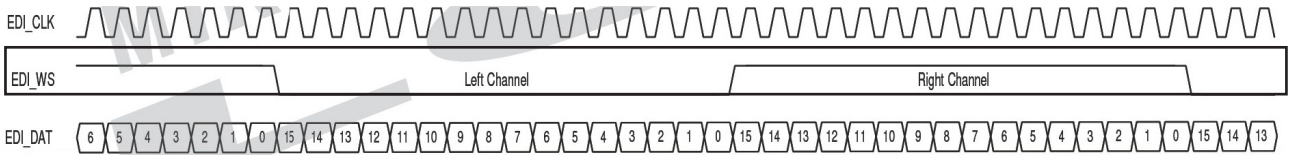


Figure 3.13.4 Block diagram of digital circuit of audio front end

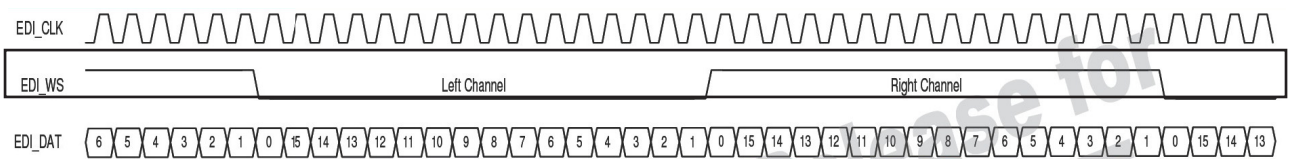


Figure 3.13.5 Block diagram of digital circuit of audio front end

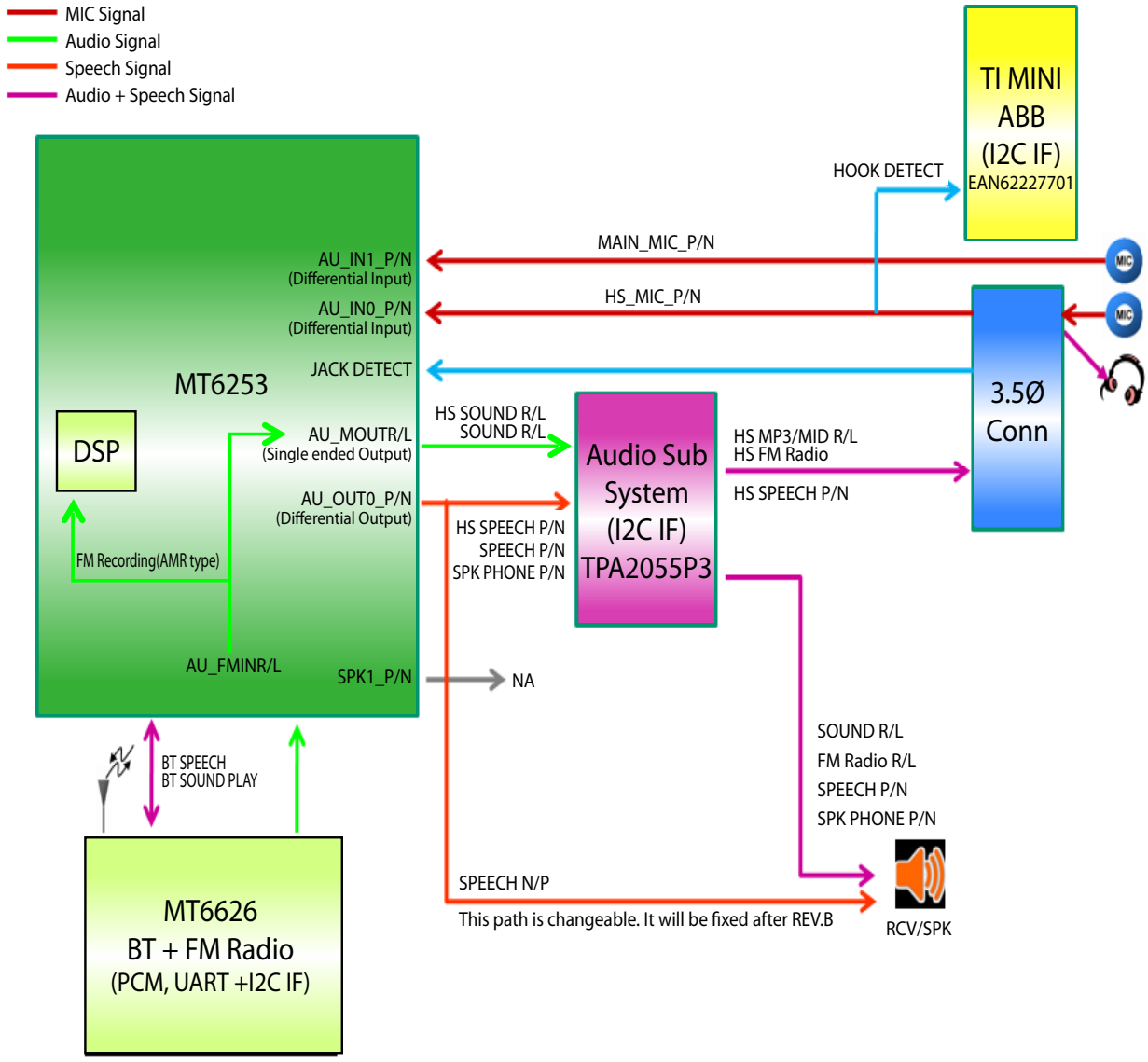
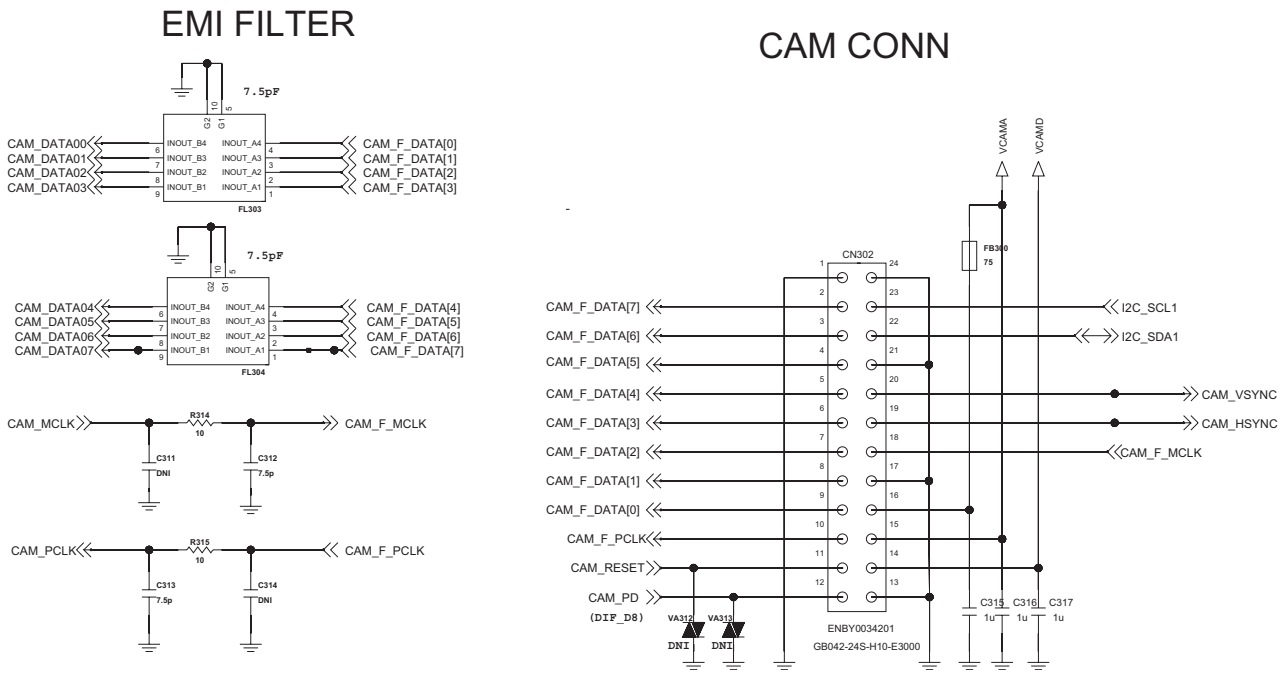


Figure 3.13.6 A290 Audio Block Diagram

3.14 Camera Interface



YACC6A1S is a high quality 1.3mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.
YACC6A1S incorporates a 1324 x 1084 pixel array, on chip 10-bit ADC, and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise, and random noise.

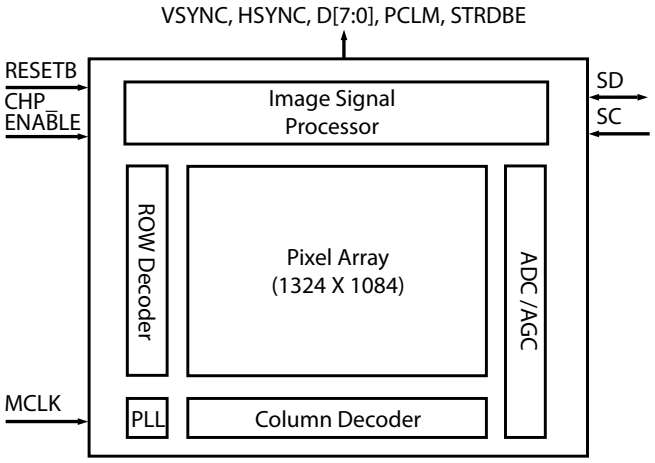


Figure 3.14.1 Camera Sensor Block Diagram

3.14.1 FEATURES

- **Pixel Size:** 1.75um X 1.75um
- **Active Image Size :** 2.296mm (H) X 1.848mm (V)
- **Resolution :** 1,280 H X 1,024 V
- **Color Filter :** RGB Bayer
- **Optical Format :** 1/6 inch
- **Frame Rate :** 20fps@SXGA, 30fps@720P, 40fps@VGA
- **Power Supply :** 2.8V / 1.8V
- **Power Consumption :** TBD @ 15fps, SXGA
- **ADC :** 10bit
- **PLL :** On Chip
- **Operation Temperature :** -20 ~ 60 ºC
- **Master Clock :** 48MHZ(Max)
- **Host Interface :** two-wire serial bus interface
- **Windowing :** Programmable
- **Output Format :** YUV4:2:2, RGB5:6:5, ITU656-like
- **Sub-Sample :** 1/2, 1/4 (VGA, QVGA)
- **Image Scaling :** 1x ~ 1/64x
- **Image Flip :** X/Y Flip
- **Auto Exposure**
- **Auto White Balance**
- **Anti-Flicker(50Hz / 60Hz) :** Auto/Manual
- **Noise Reduction**
- **Black Level Calibration**
- **Stobe Control :** Support Xenon / LED Type
- **On-Chip Dead Pixel Correction**
- **Edge Enhancement**
- **Brightness**
- **Color Saturation**
- **Gamma Correction**
- **Color Correction**
- **Lens Shading Correction**
- **Image Effect :** Mono, Sepia, Solarization, Negative, Sketch, Embossing

Figure 3.14.2 Camera Sensor features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	VDD:D	1.7	1.8	1.9	V	
Analog Circuit Power Supply Voltagey	VDD:A	2.7	2.8	3.0	V	
Analog Pixel Circuit Power Supply Voltagey	VDD:P	2.7	2.8	3.0	V	
Digital I/O Circuit Power Supply Voltagey	VDD:I	1.7	1.8/2.8	3.0	V	
H level Input Voltage	VIH	0.7*$V_{DD:I}$			V	
L level Input Voltage	VIL			0.3*$V_{DD:I}$	V	
Output High Current (VDD:I=2.8V, VOH=2.4V)	IOH		4.2		mA	1
Output High Current (VDD:I=1.8V, VOH=1.4V)	IOH		3.0		mA	1
Output Low Current (VDD:I=2.8V, VOH=0.4V)	IOL		4.8		mA	1
Output Low Current (VDD:I=1.8V, VOH=0.4V)	IOL		3.8		mA	1

Note1) User can control the amount of current by controlling bit[7:3] of PWRCTL[0x01:P0].
Above valuse are ouput current when bit[7:3] of PWRCTL[0x01:P0] is 5'b01010.

Figure 3.14.3 Camera Sensor DC charicteristics

3.15 KEY BACLKLIGHT LED Interface

Key Backlight LED is controlled by KEYPAD_LED signal of MT6253.
The built-in open drain output switch drives the Keypad LED in the handset. This switch is controlled by baseband with the enable register. The keypad LED can sink 150mA and will become high impedance as disabled.

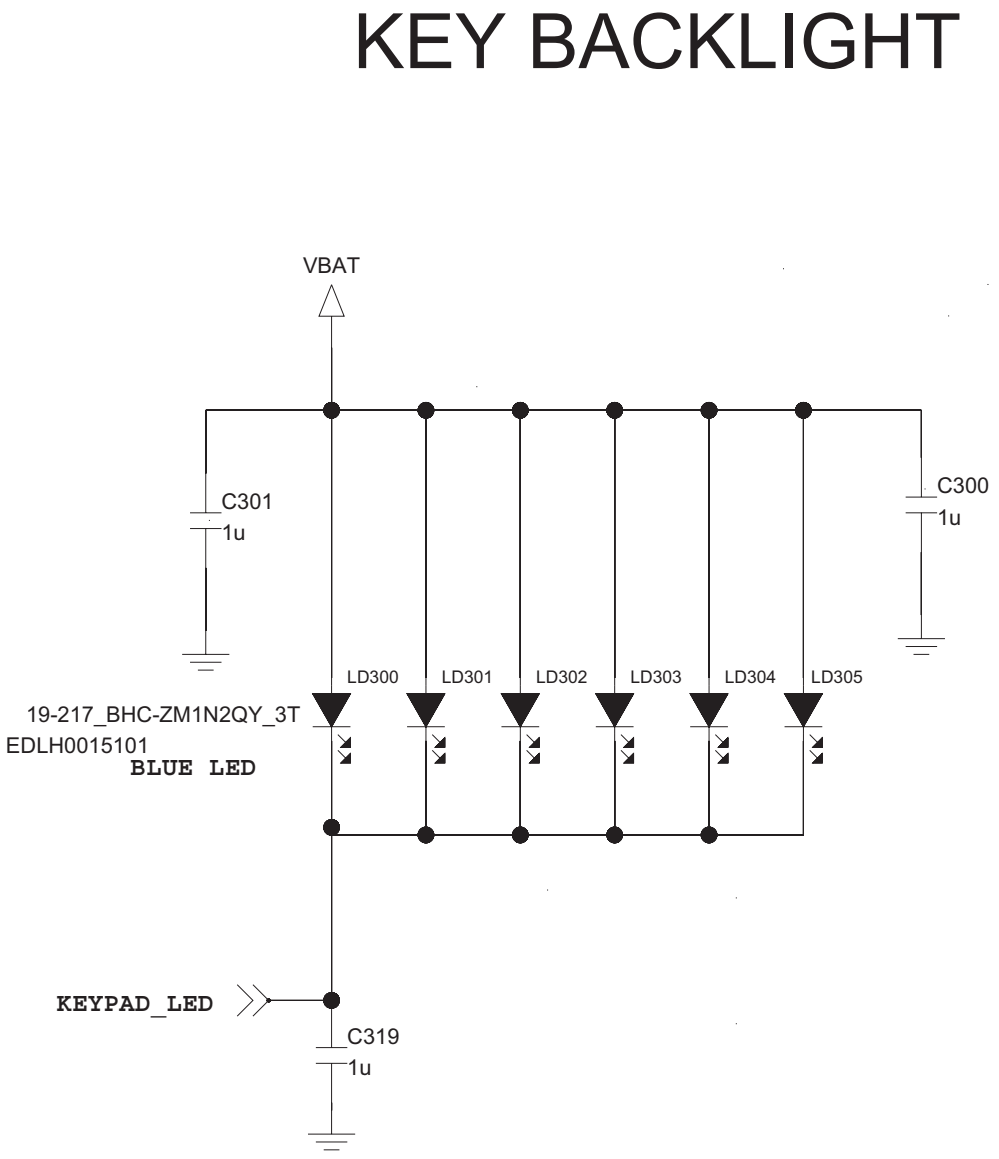


Figure 3.15.1 Key Backlight Block

3.16 Vibrator Interface

Vibrator is driven by MINI ABB LDO source.
VIB_3V3 is connected with + terminal of vibrator and – terminal is connected with GND. It is controlled by source of MINI ABB(only ON/OFF function).
MINI ABB is controlled by I2C IF of MT6253.

VIBRATOR

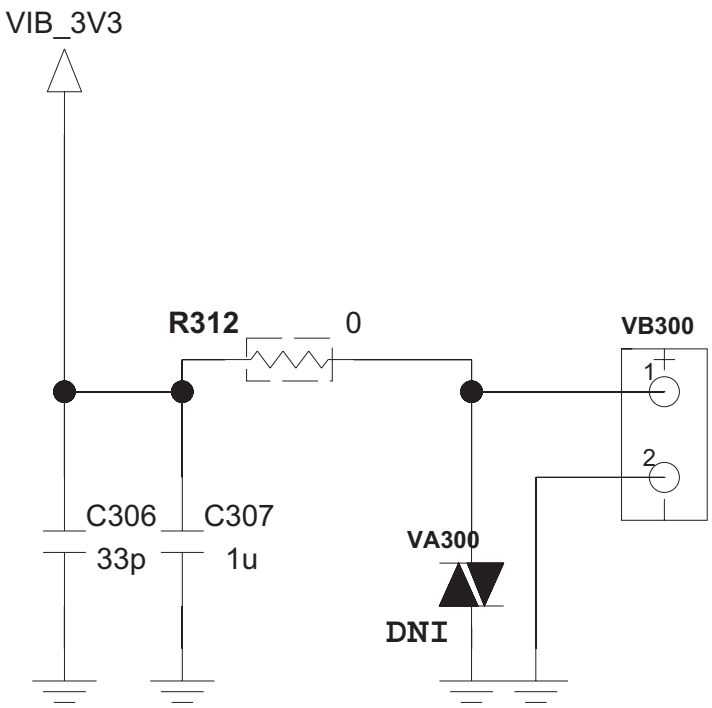


Figure 3.16.1 Vibrator Driver Block

3.17 Torch LED Interface

Torch LED is driven by MINI ABB LDO source.
TORCH_3V3 is connected p-channel of LED.It is controlled by source of MINI ABB(only ON/OFF function).
MINI ABB is controlled by I2C IF of MT6253.

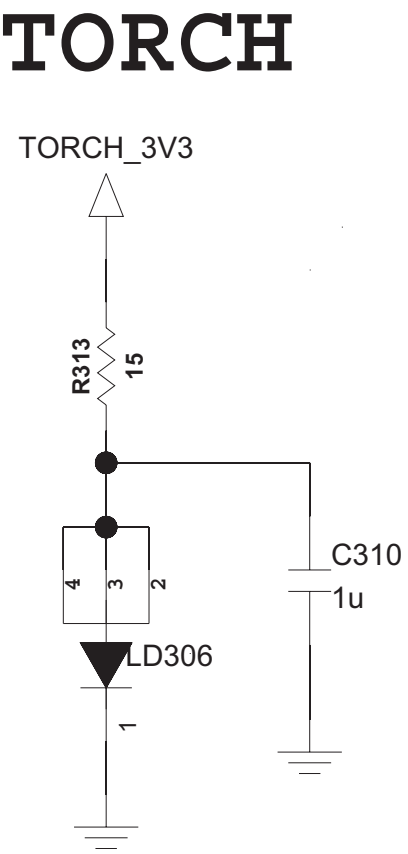
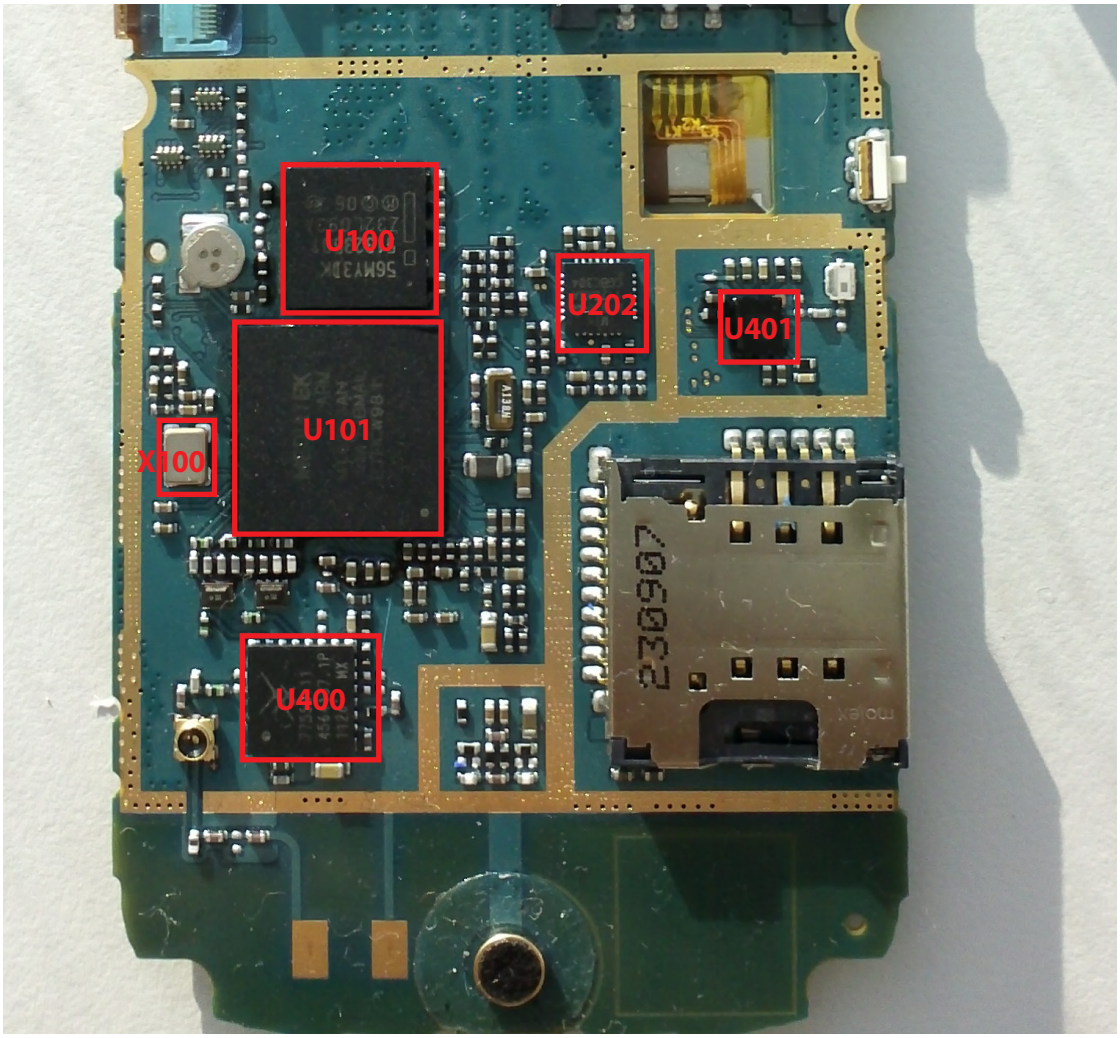


Figure 3.17.1 Torch Driver Block

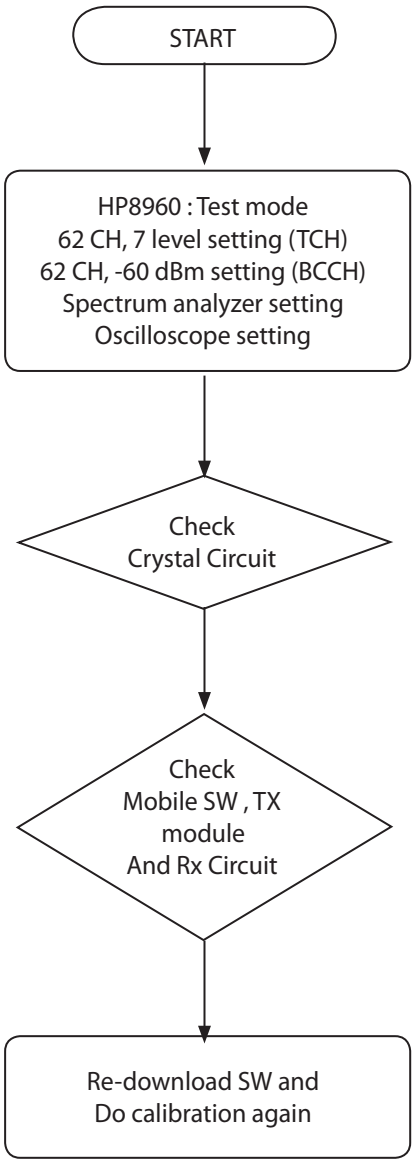
4. TROUBLE SHOOTING

4.1 RF Component

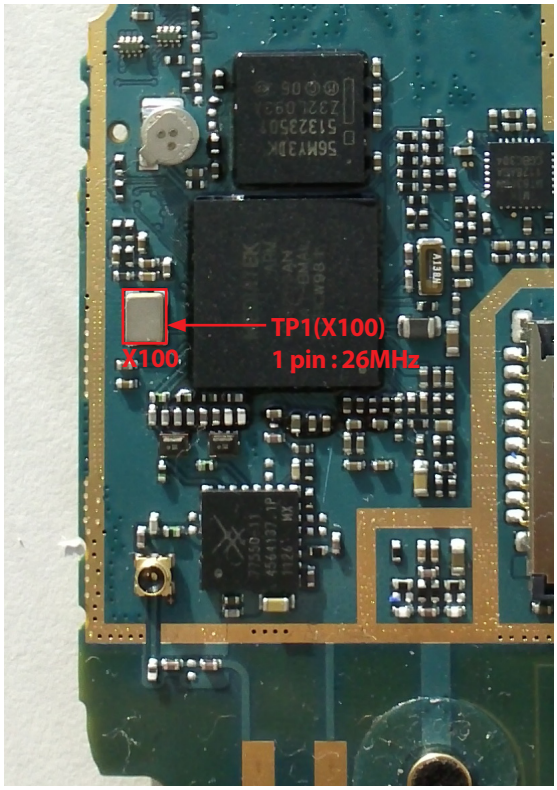


U100	Memory(256NOR/648pSDRAM) PF38F4050M0Y3DF
U101	Main Chip (MT6253)
U401	BT/FM combo chip (MT6626)
U400	TX Module (SKY77550)
X100	Crystal, 26MHz Clock
U202	SIM Switch(MT6306)

4.2 RX Trouble



(1) Checking Crystal Circuit



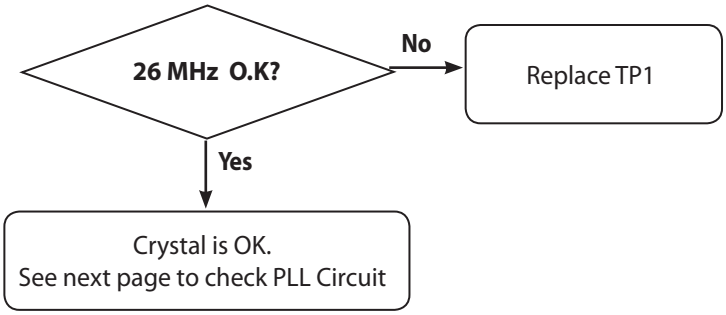
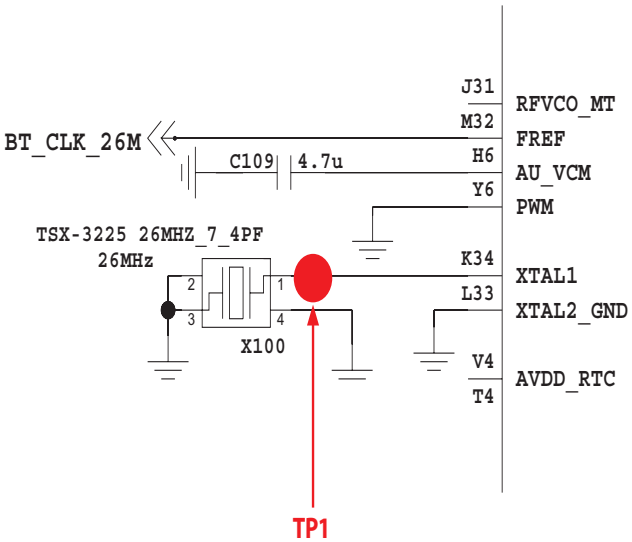


Figure 4.2.1



(2) Checking Mobile SW &Tx module

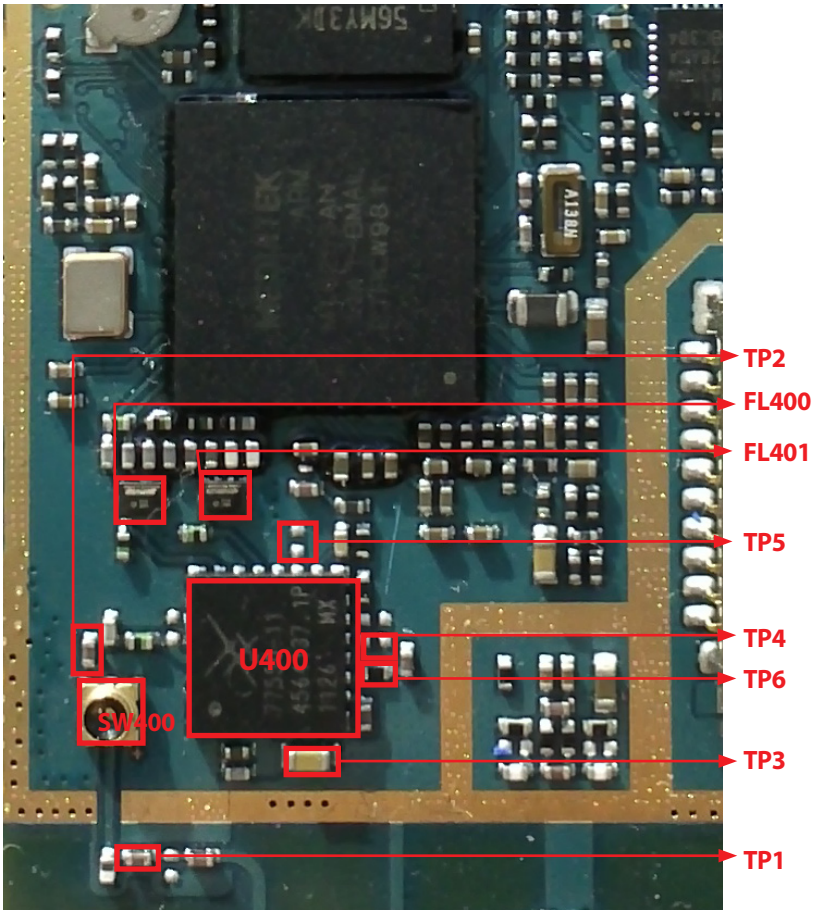
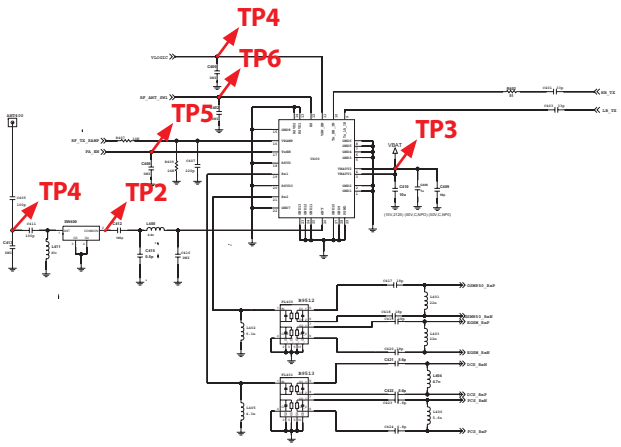
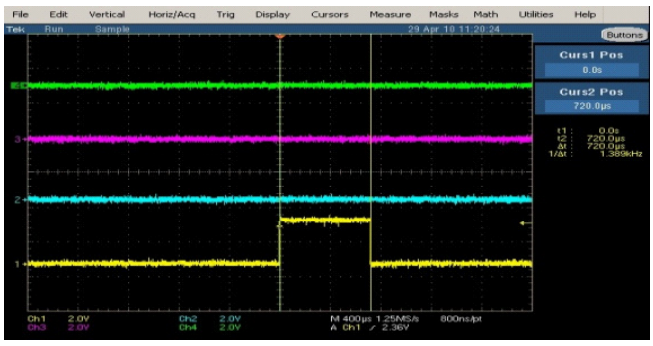
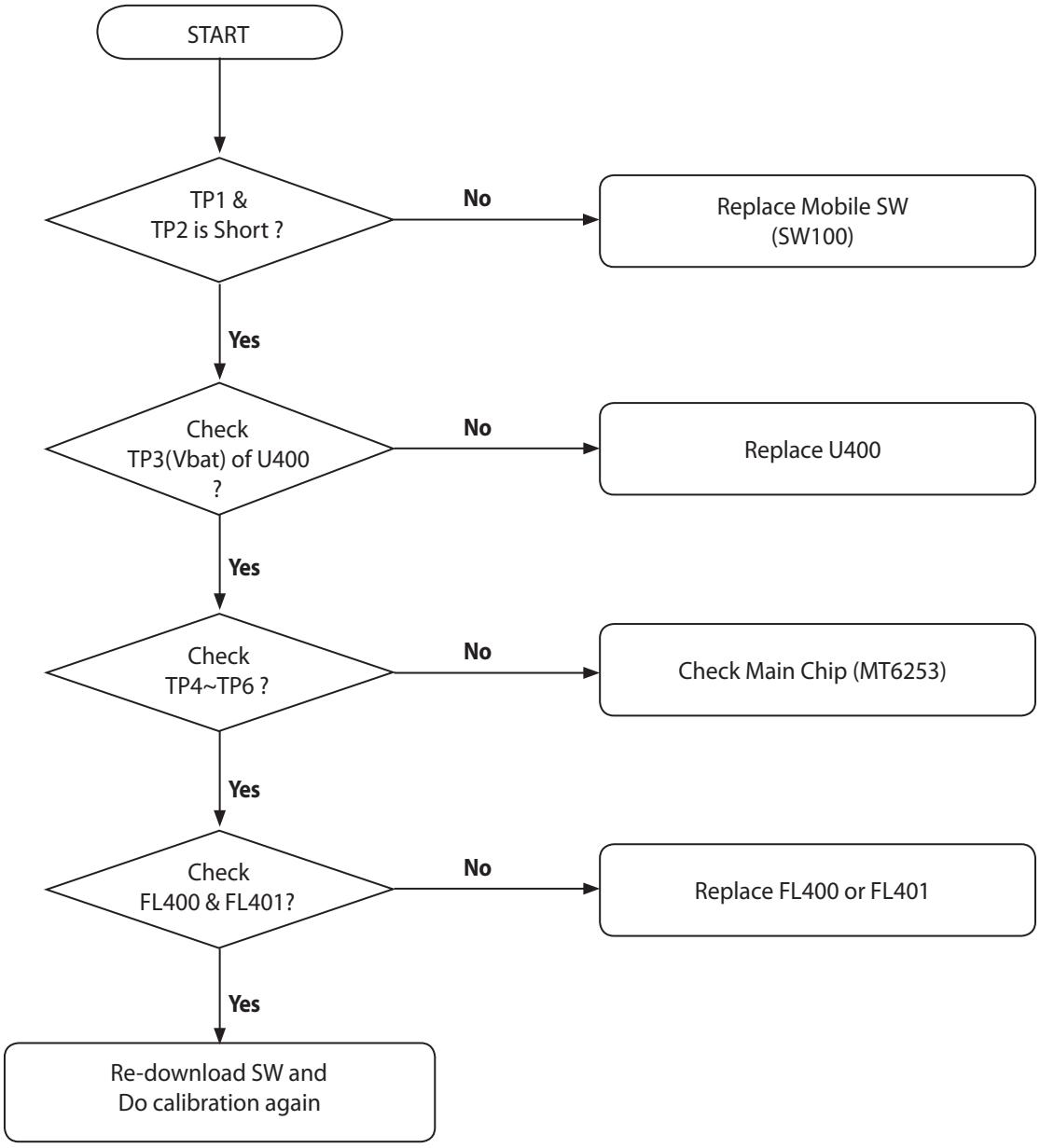


Figure 4.2.2

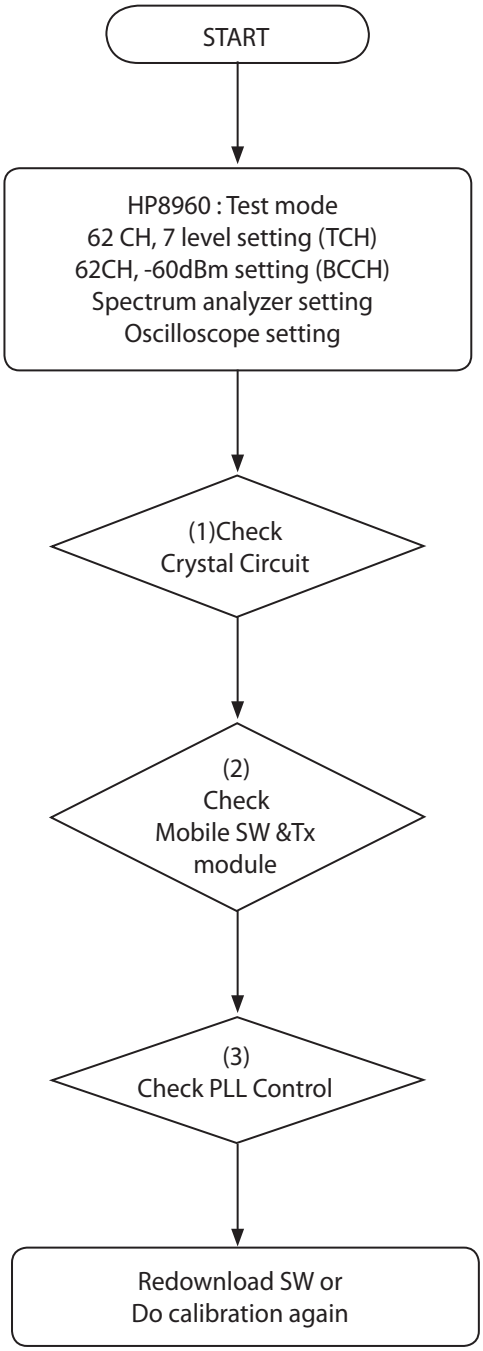




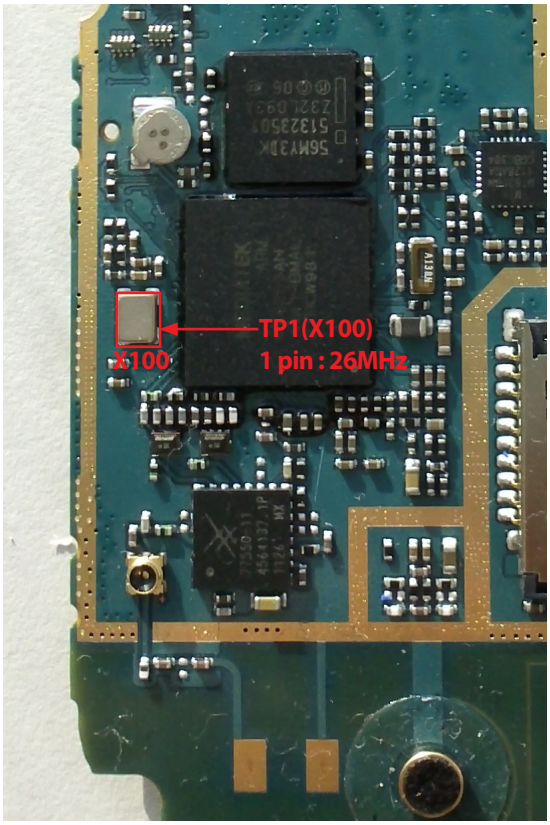


	TP4	TP5	TP6
MODE	RF_VLOGIC	RF_TX_EN	RF_BS
Stanby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

4.3 TX Trouble



(1) Checking Crystal Circuit



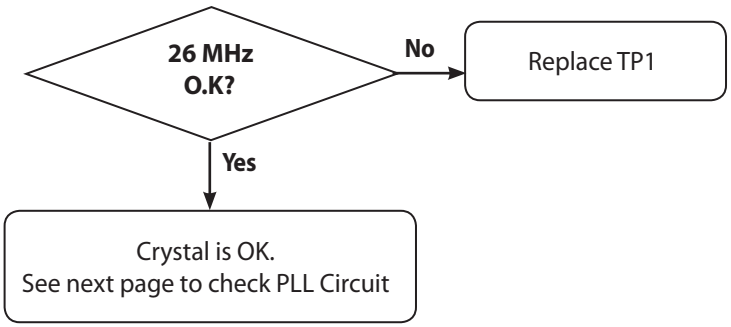
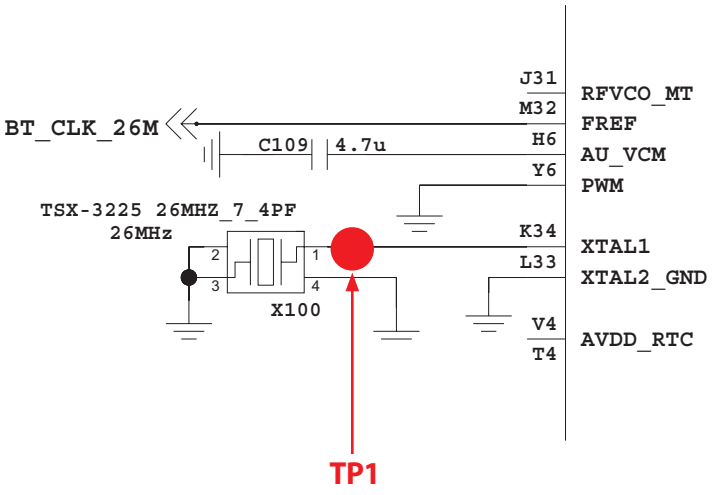


Figure 4.2.1



(2) Checking Mobile SW &Tx module

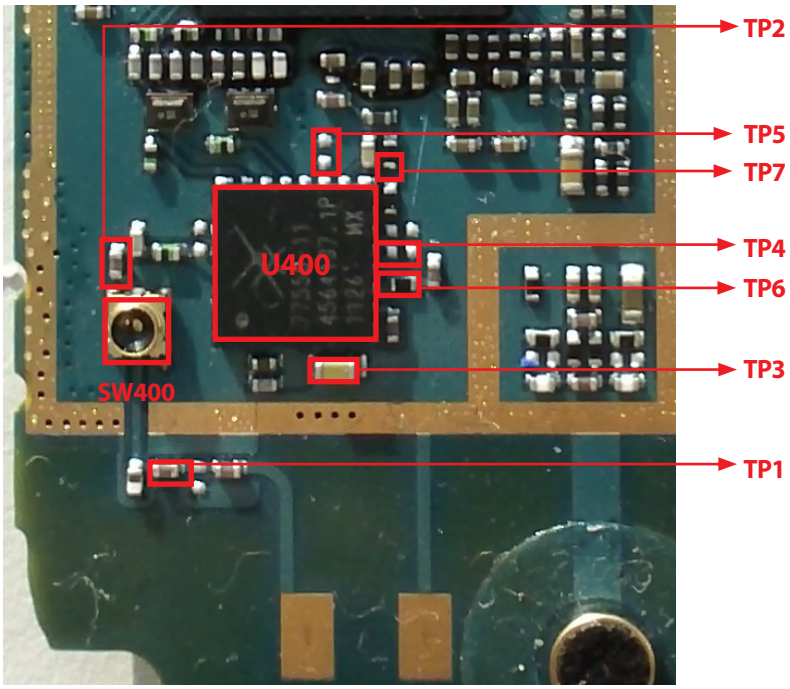
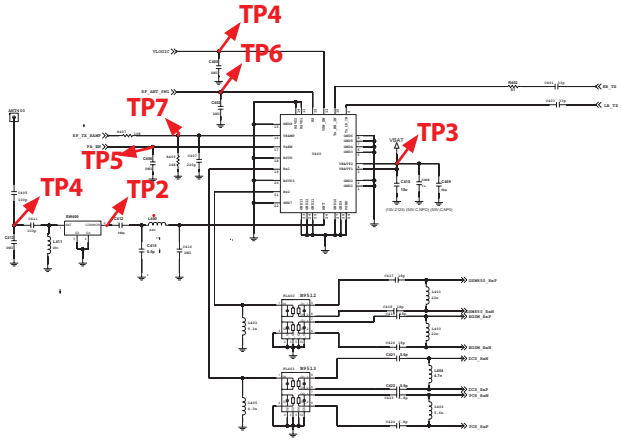
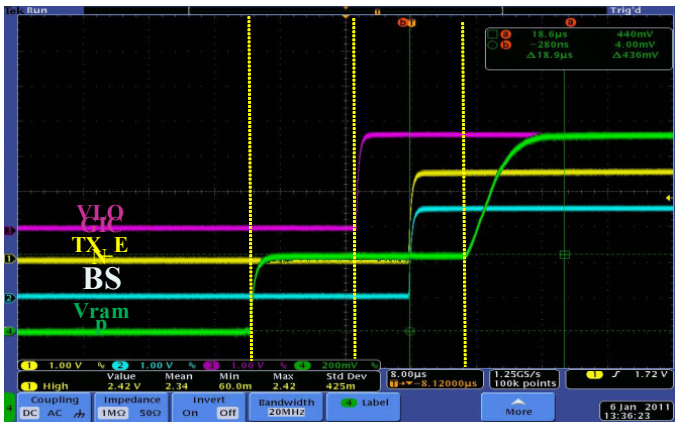
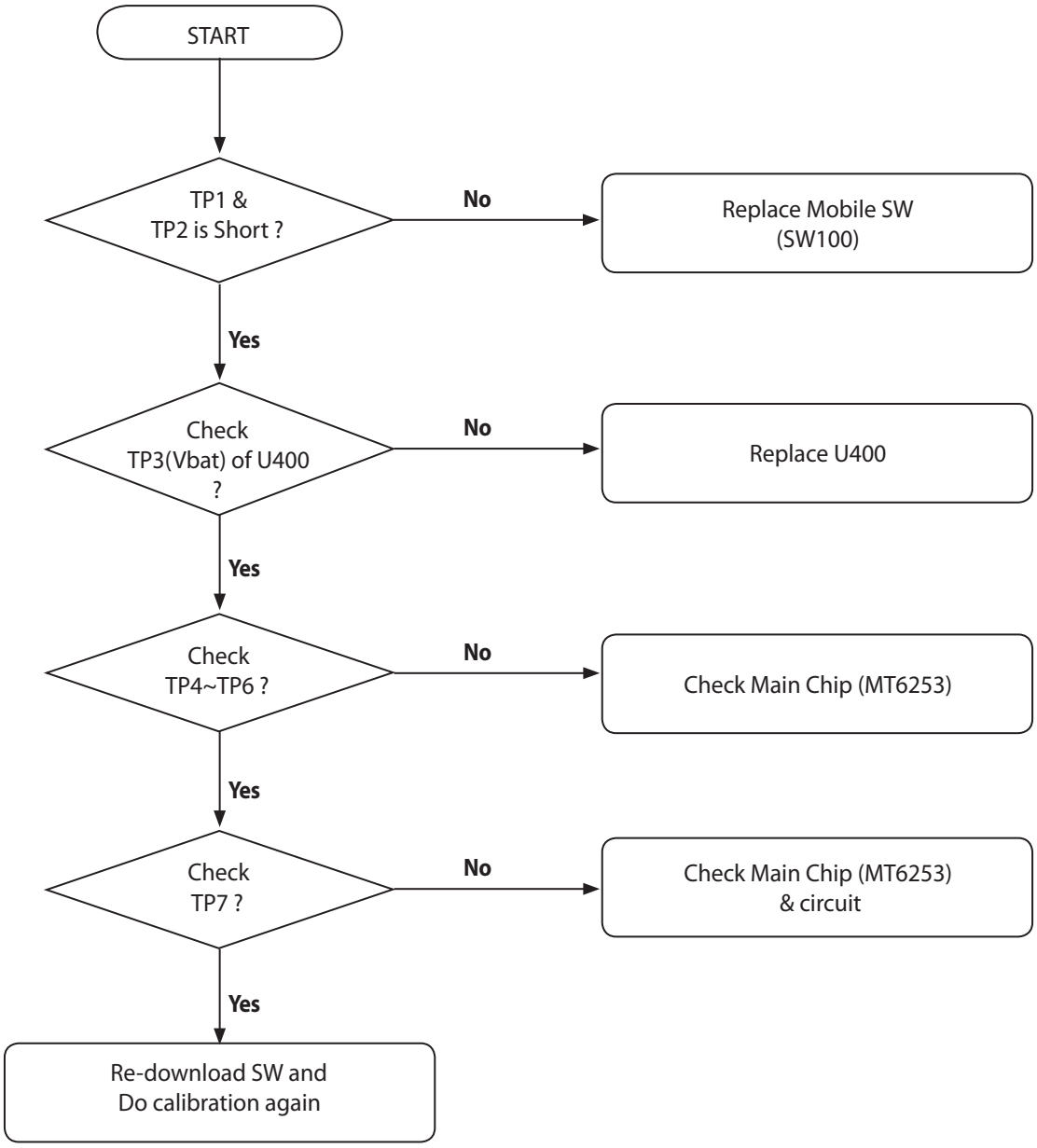


Figure 4.2.2







	TP4	TP5	TP6
MODE	RF_VLOGIC	RF_TX_EN	RF_BS
Stanby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

4.4 Power On Trouble

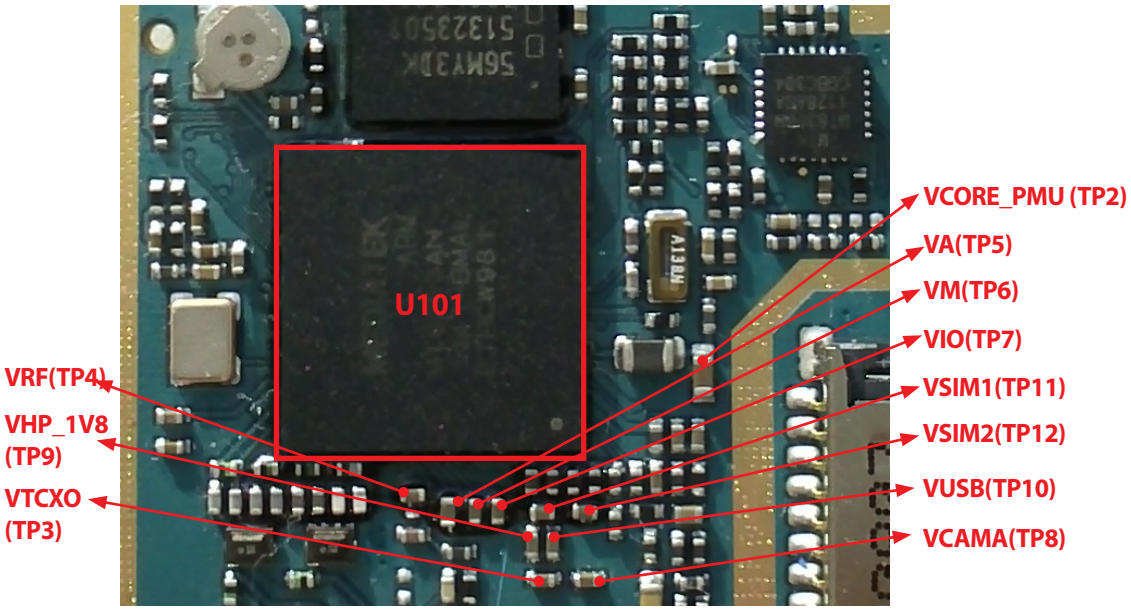


Figure 4.4.1

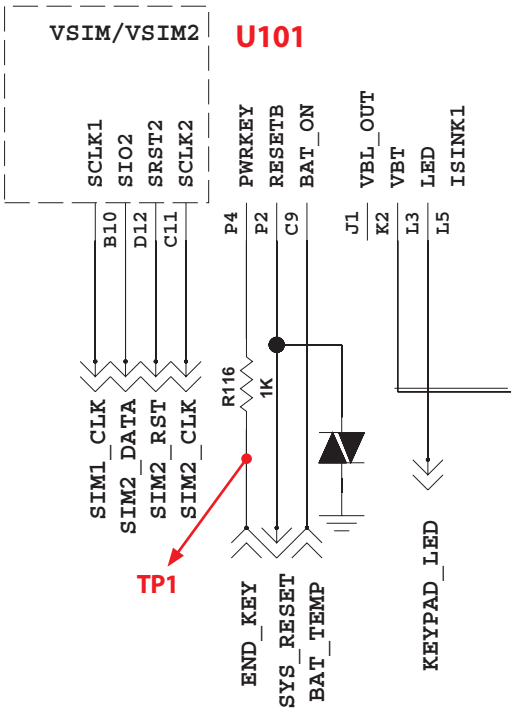


Figure 4.4.3 Remote power on

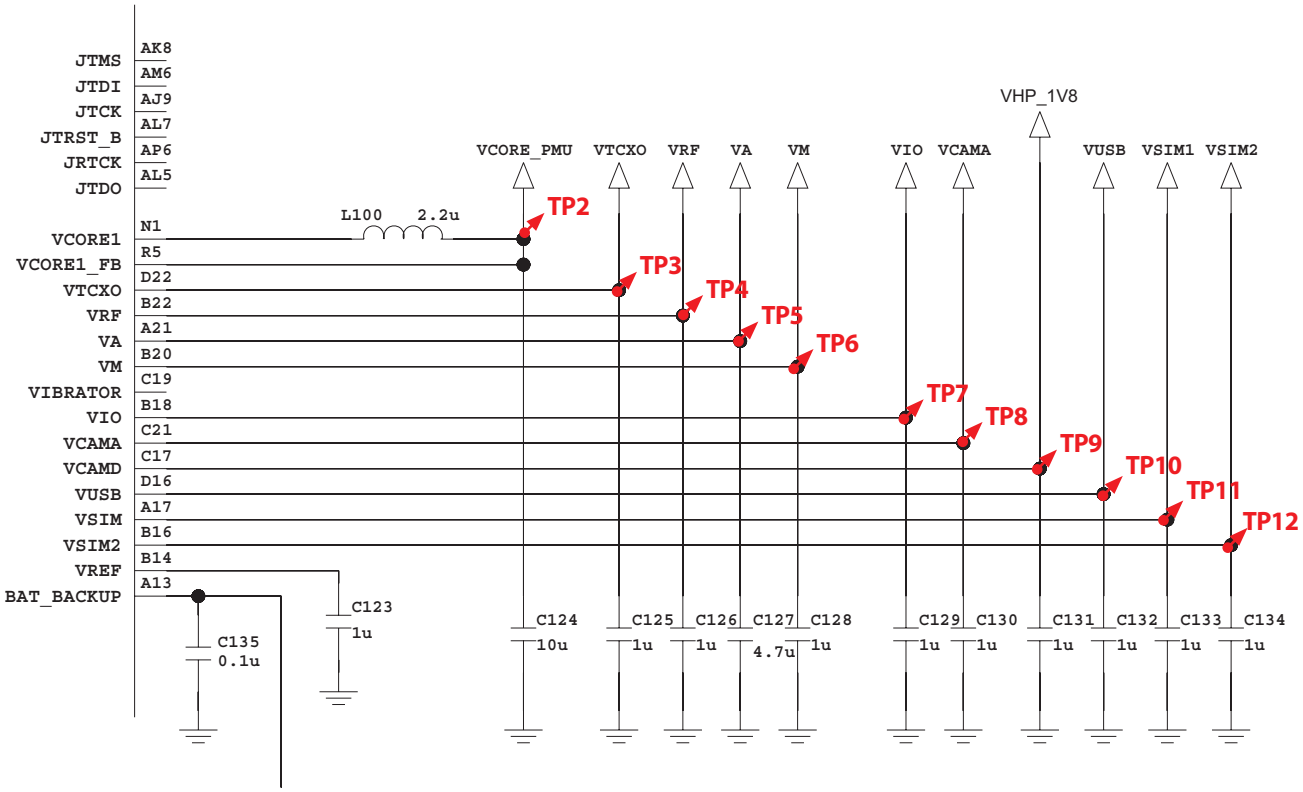
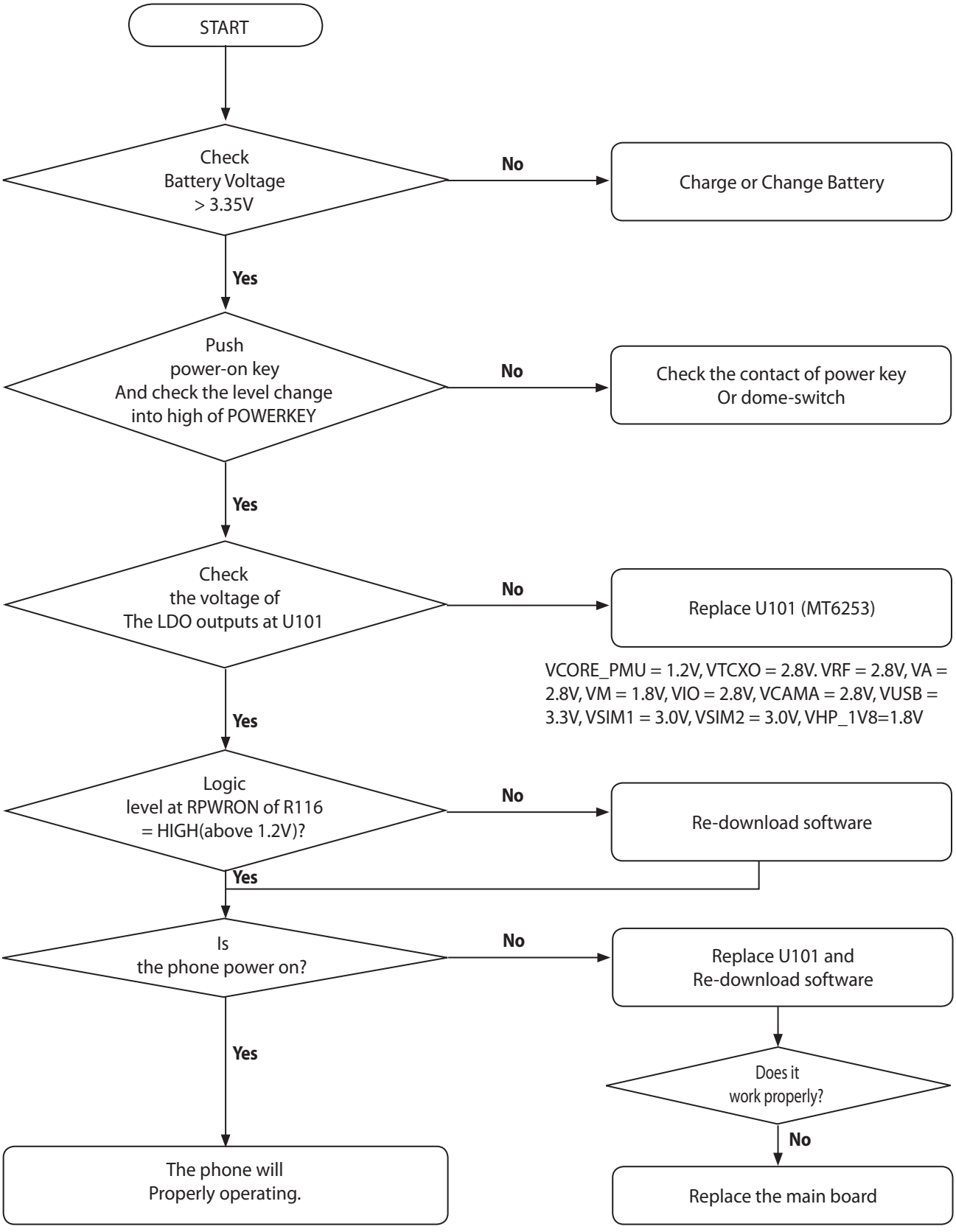


Figure 4.4.4 Power Block of LG-A290



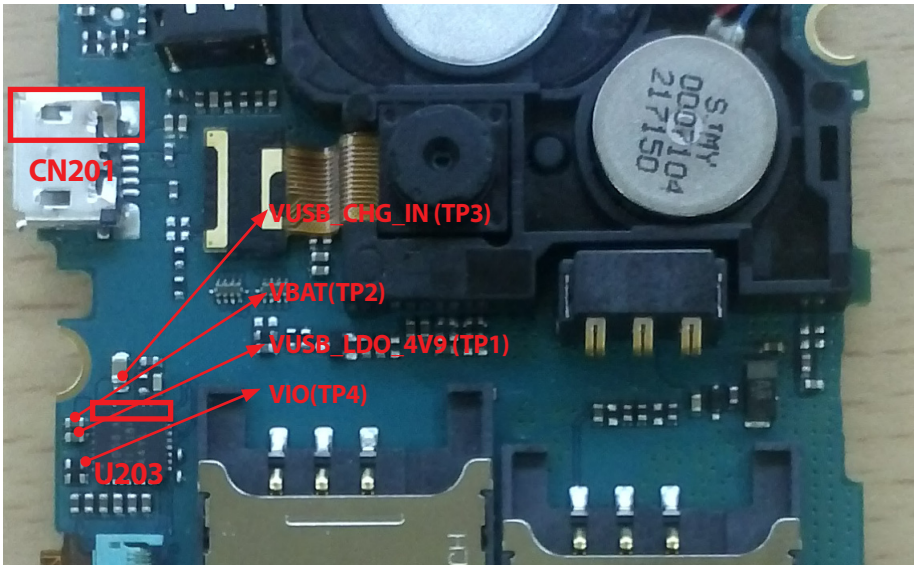


Figure 4.5.1

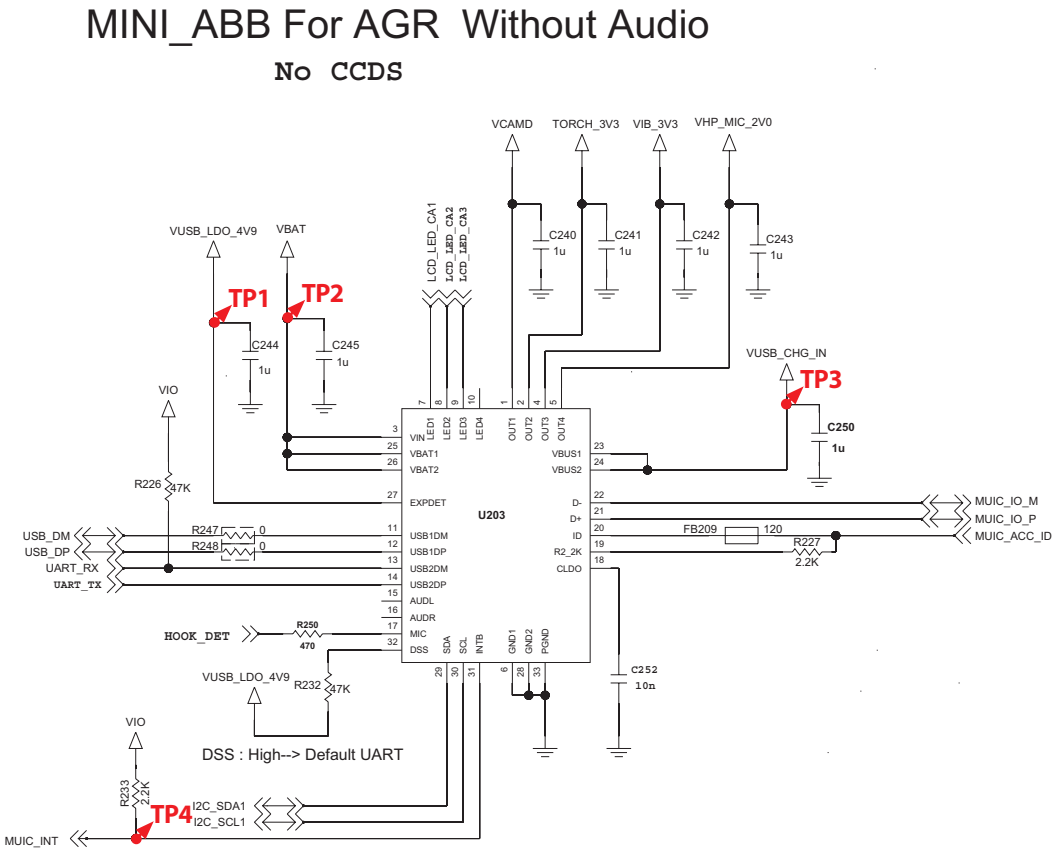
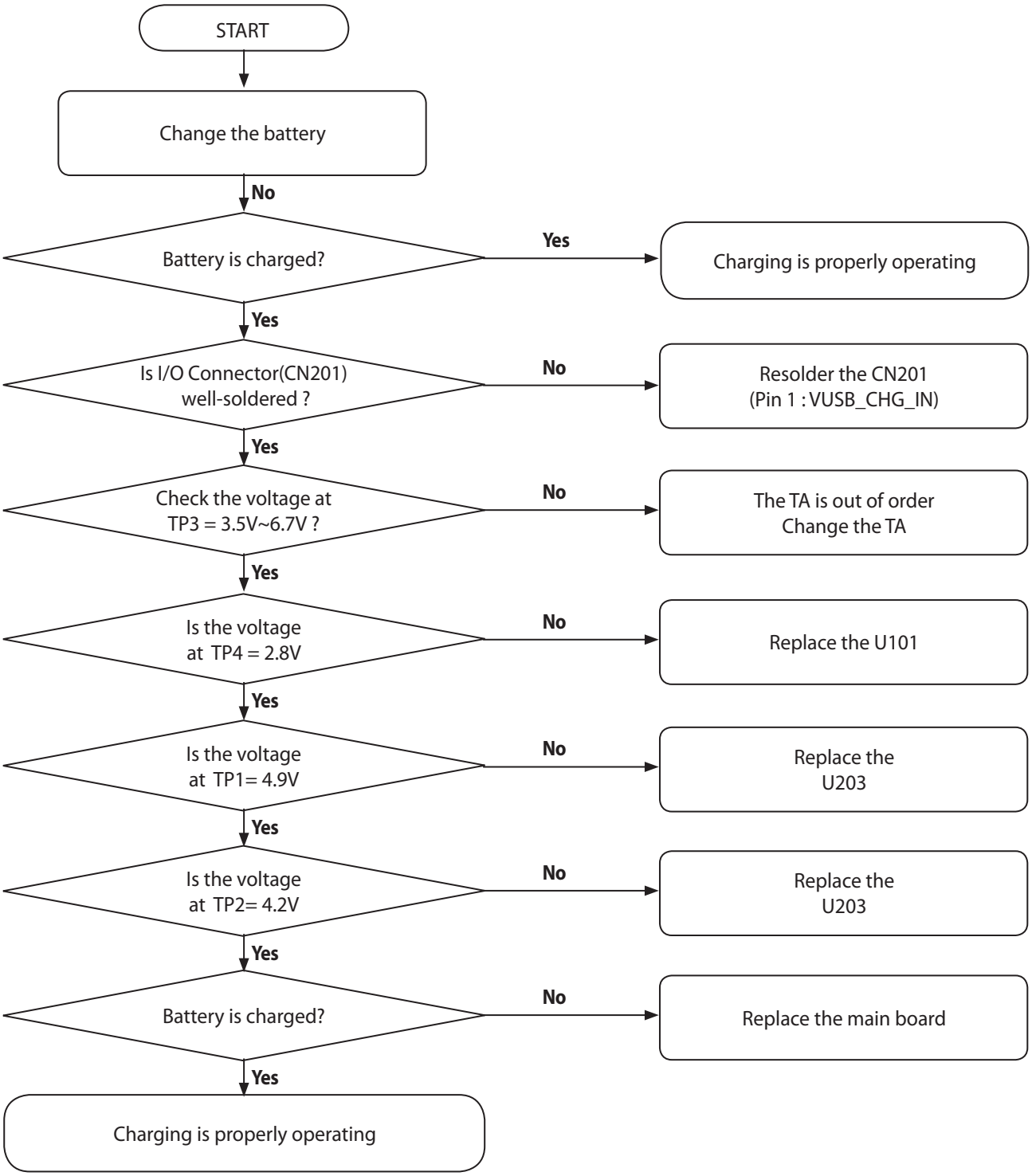


Figure 4.5.2



4.6 Vibrator Trouble

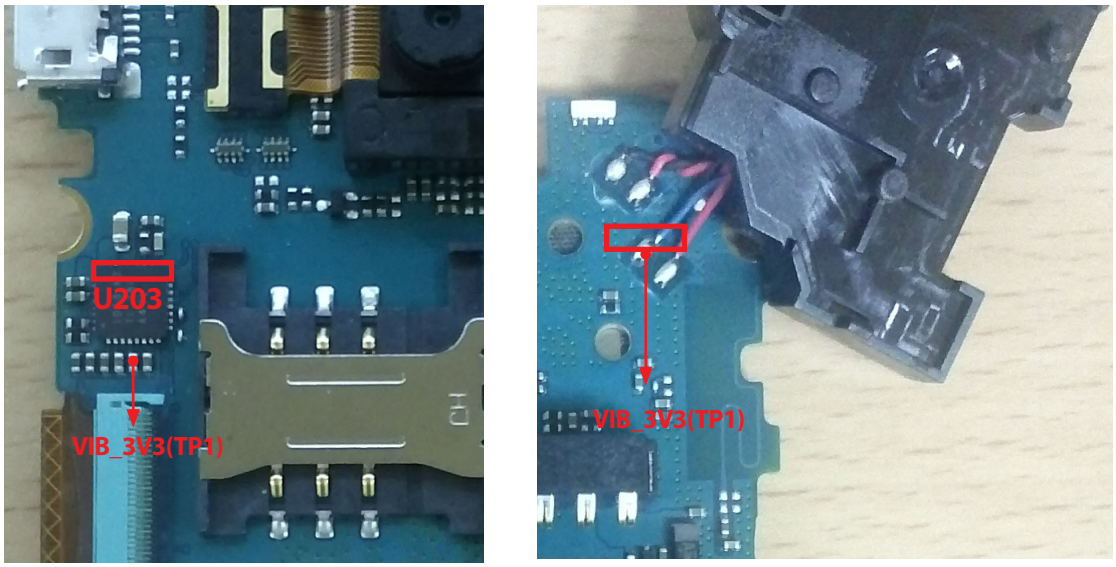


Figure 4.6.1

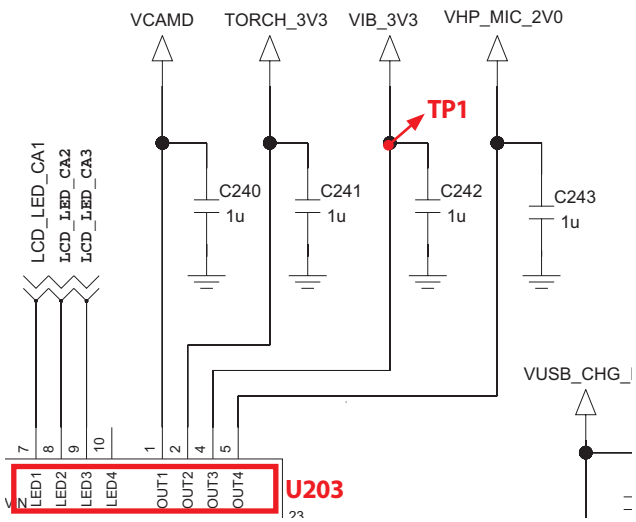


Figure 4.6.2

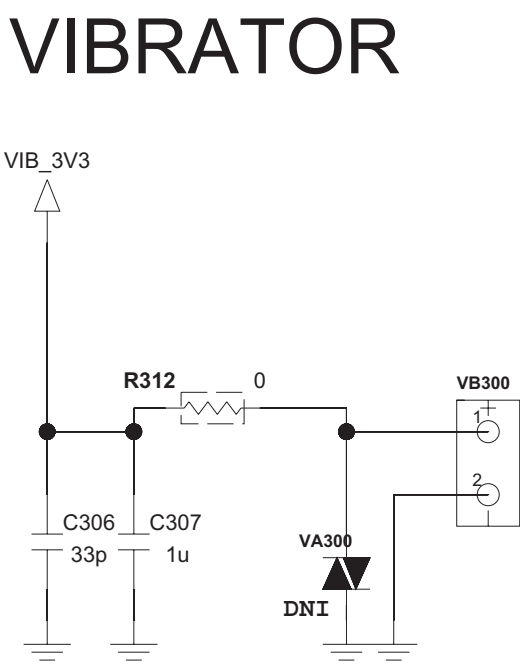
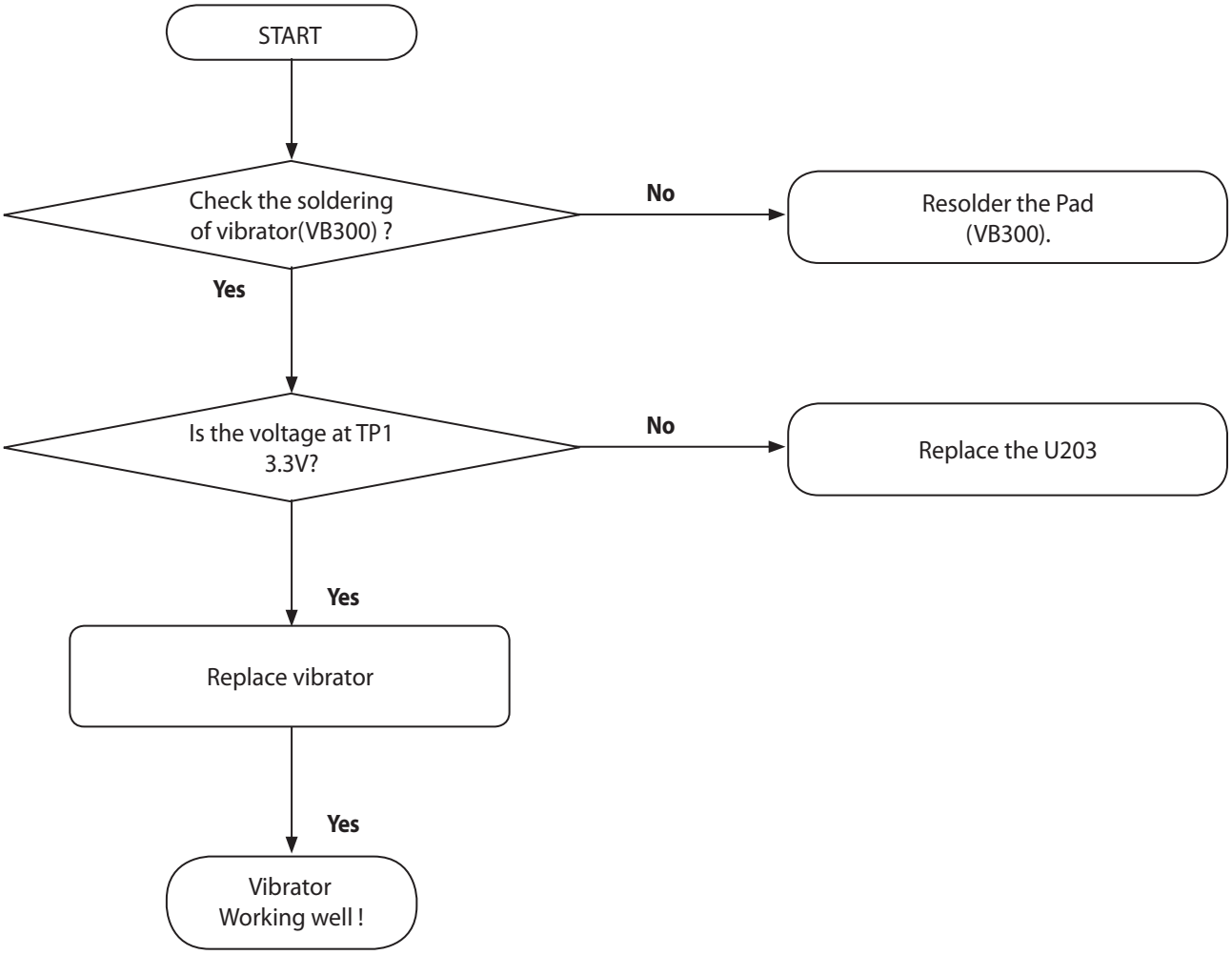


Figure 4.6.3

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

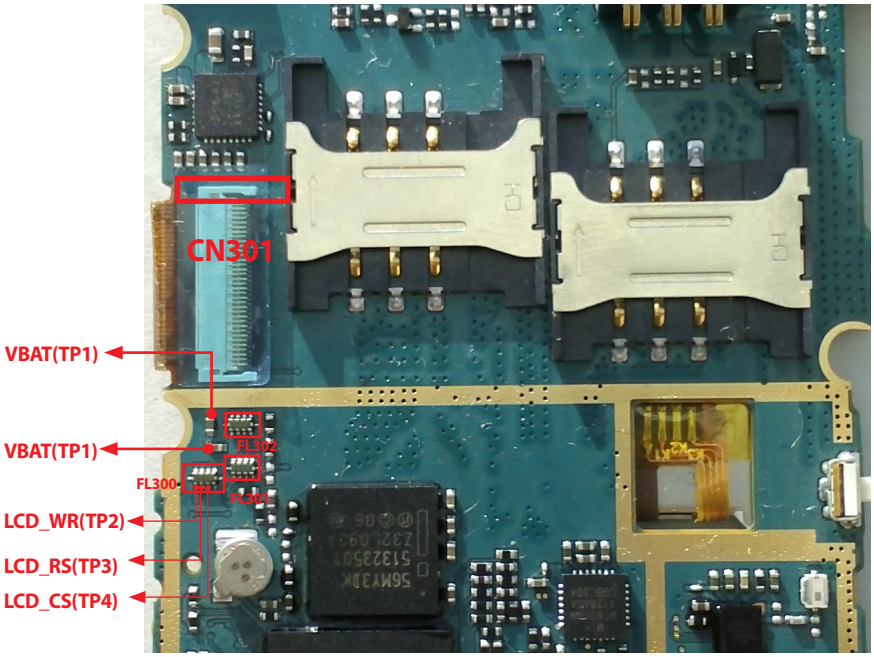


Figure 4.7.1

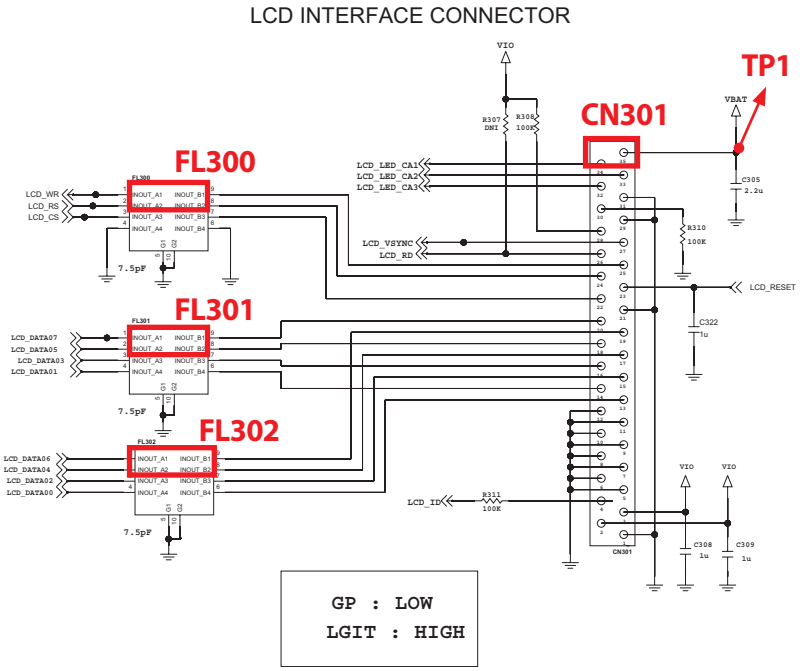
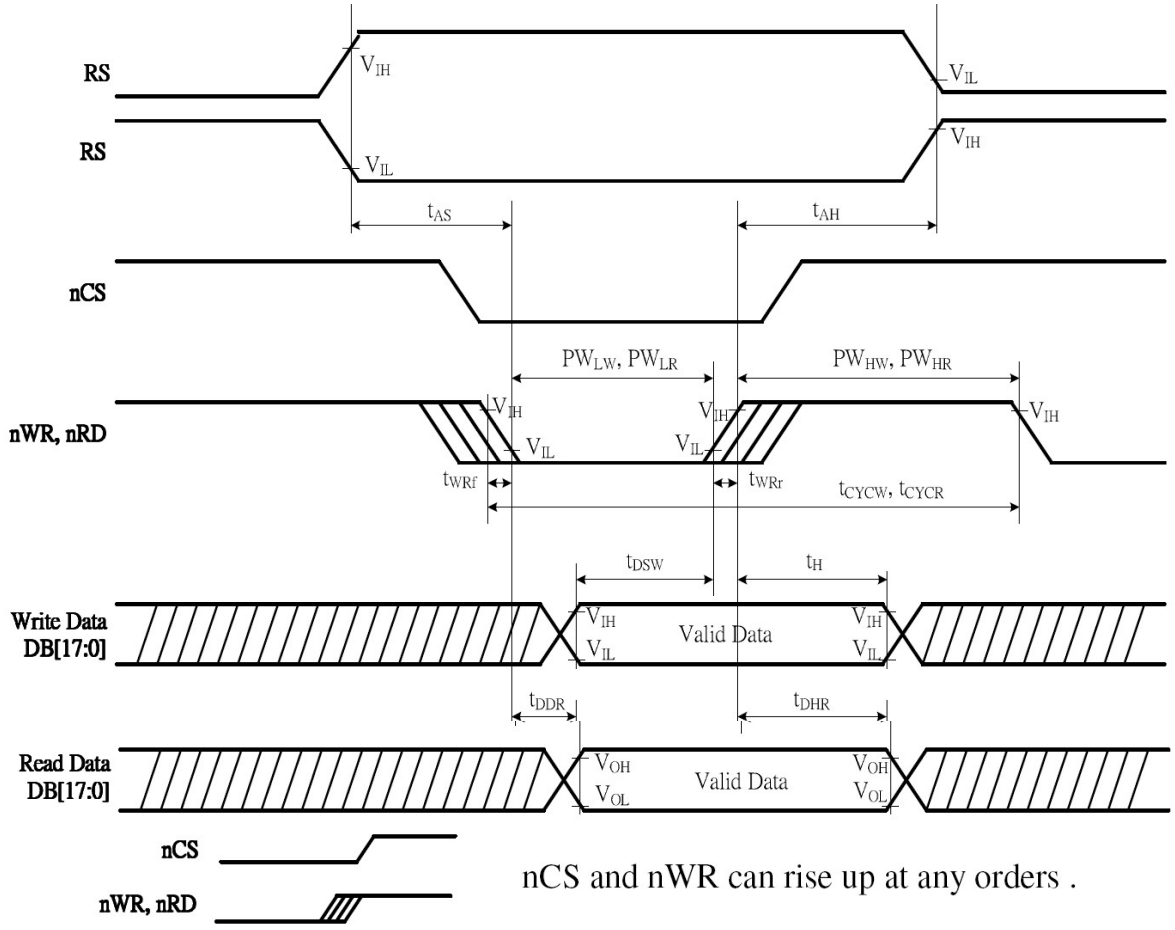
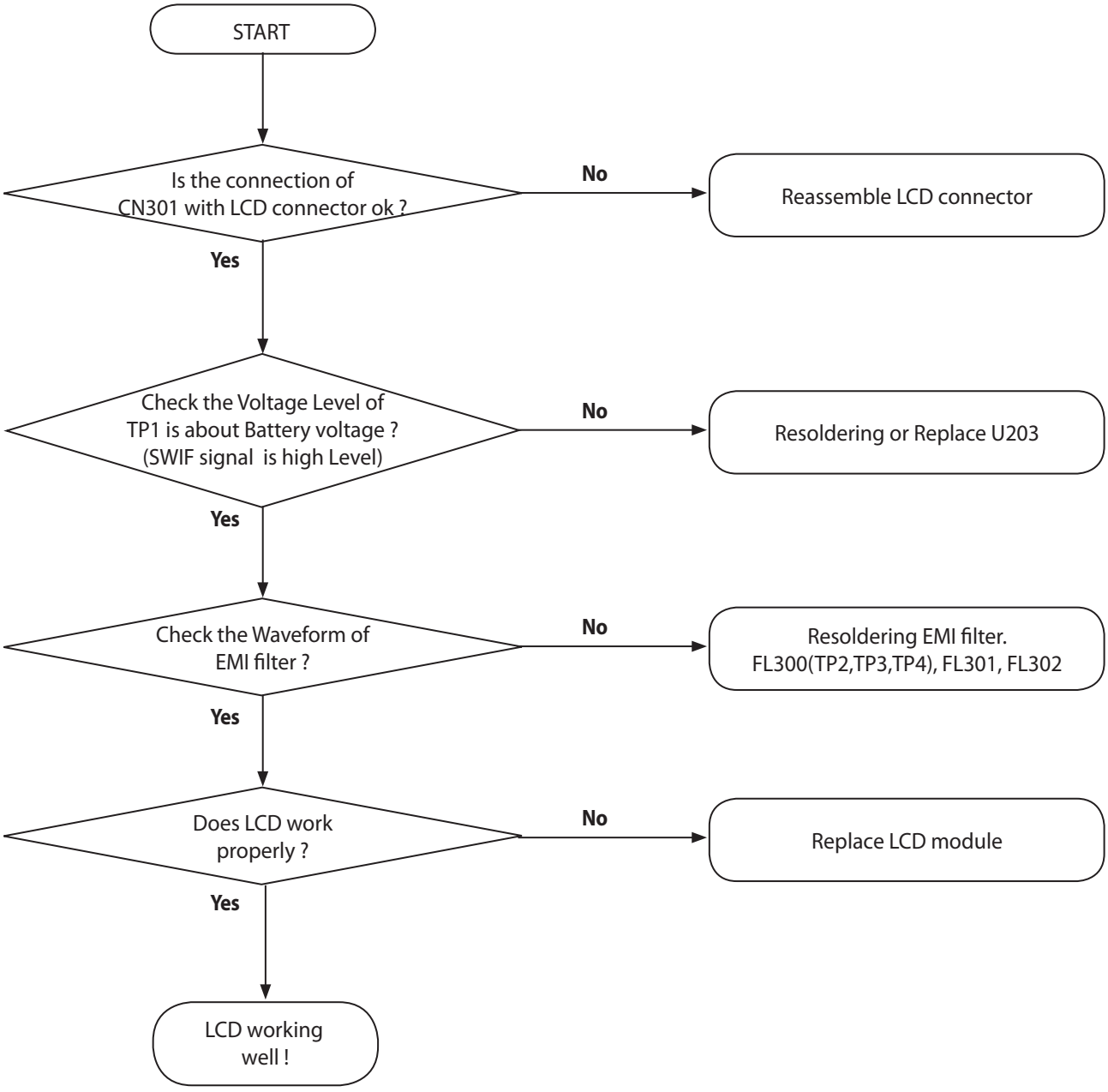


Figure 4.7.2





4.8 Camera Trouble

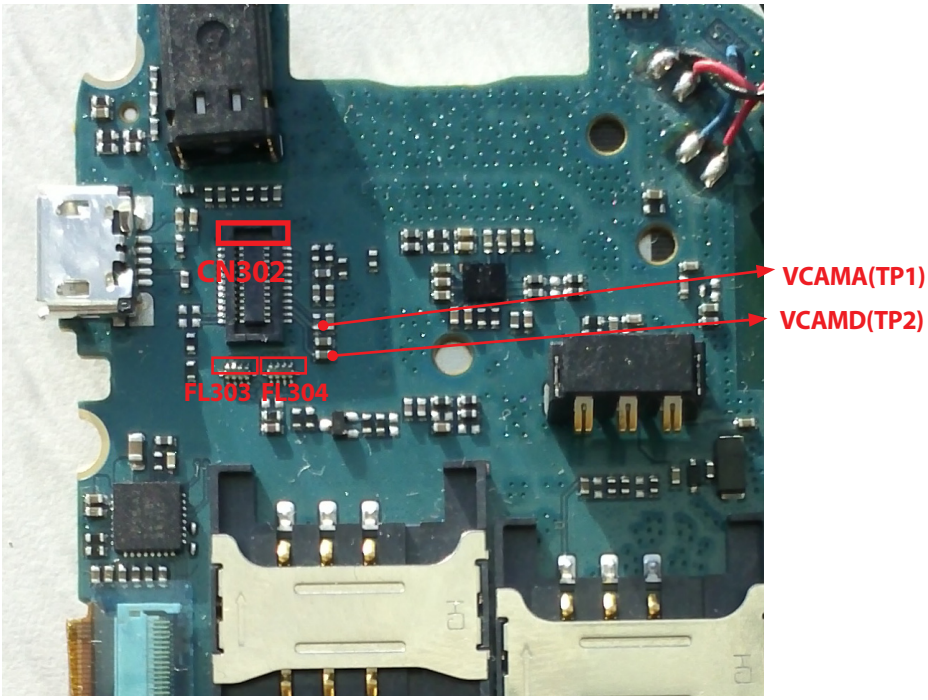


Figure 4.8.1

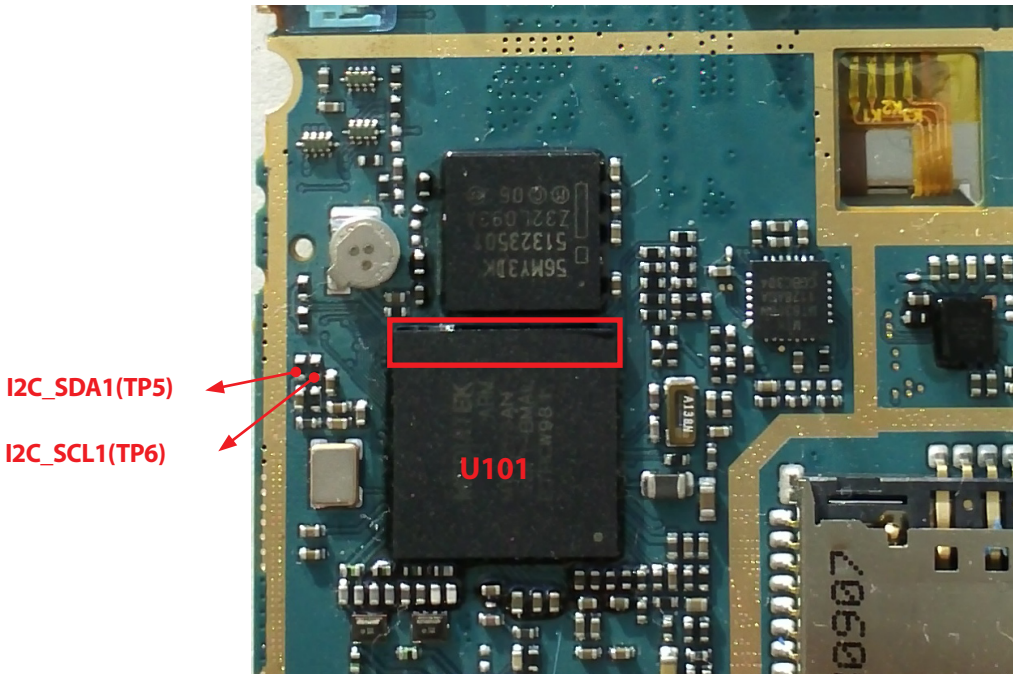
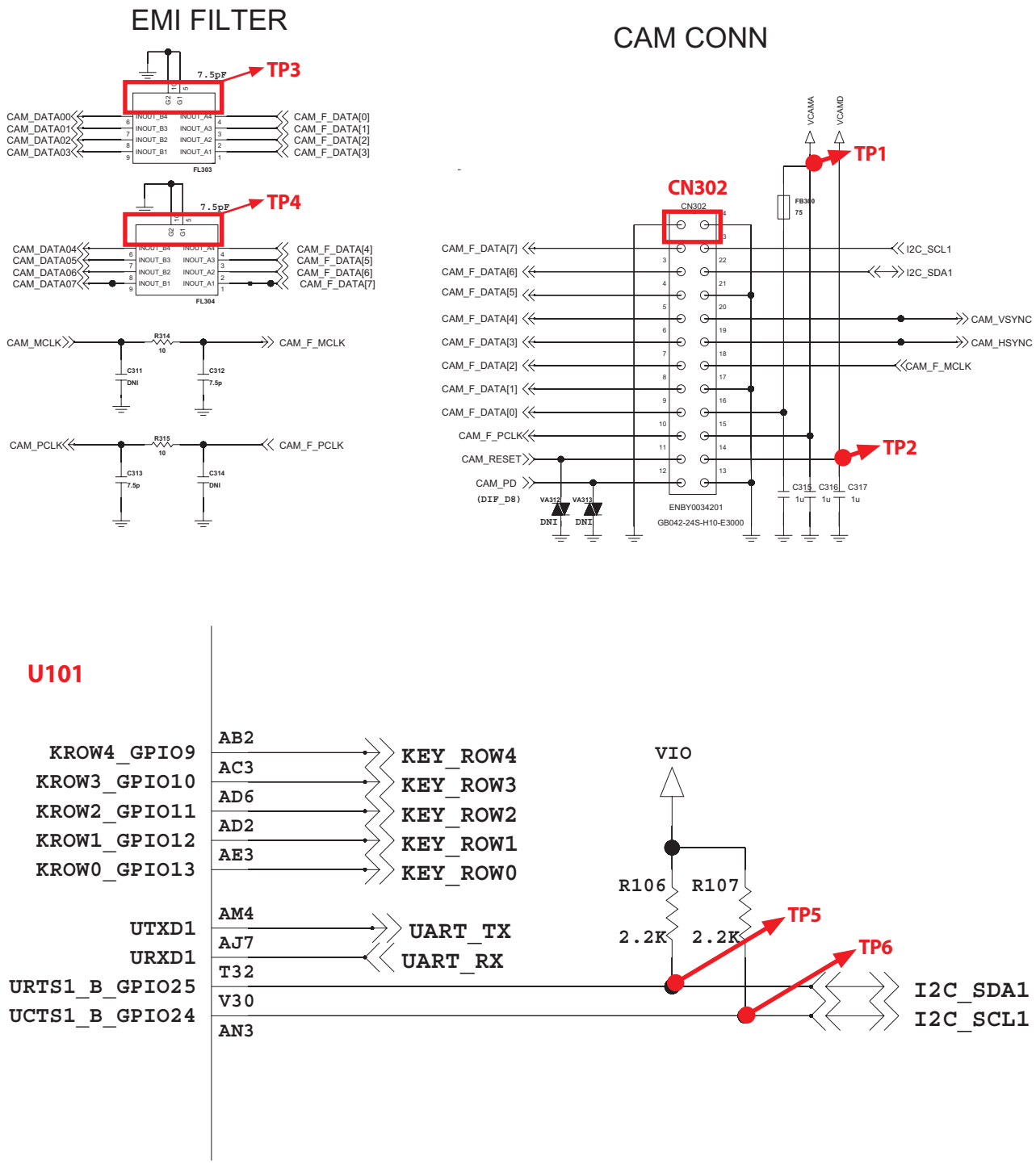
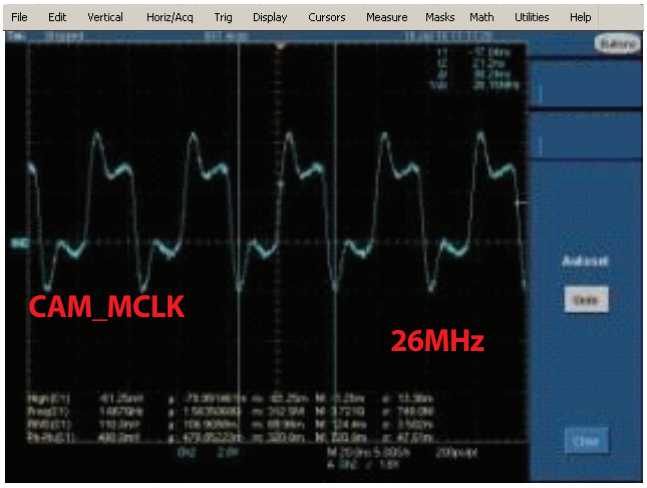


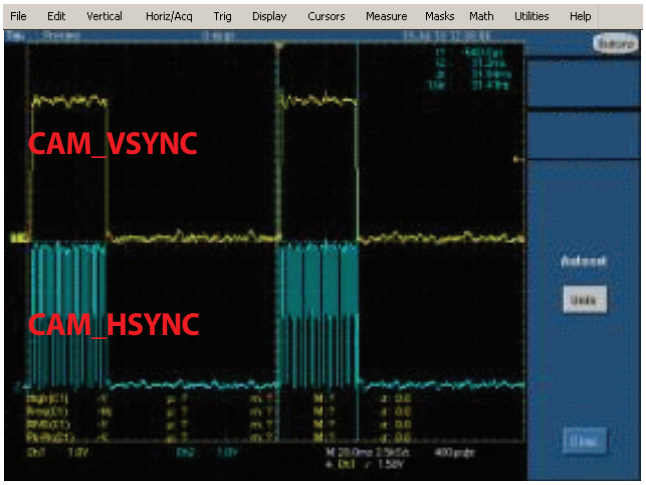
Figure 4.8.2



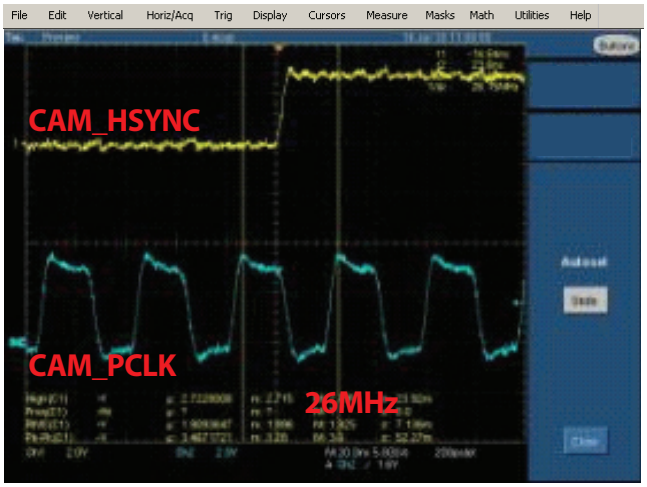
Graph 4.8.1. I2C Data Waveform



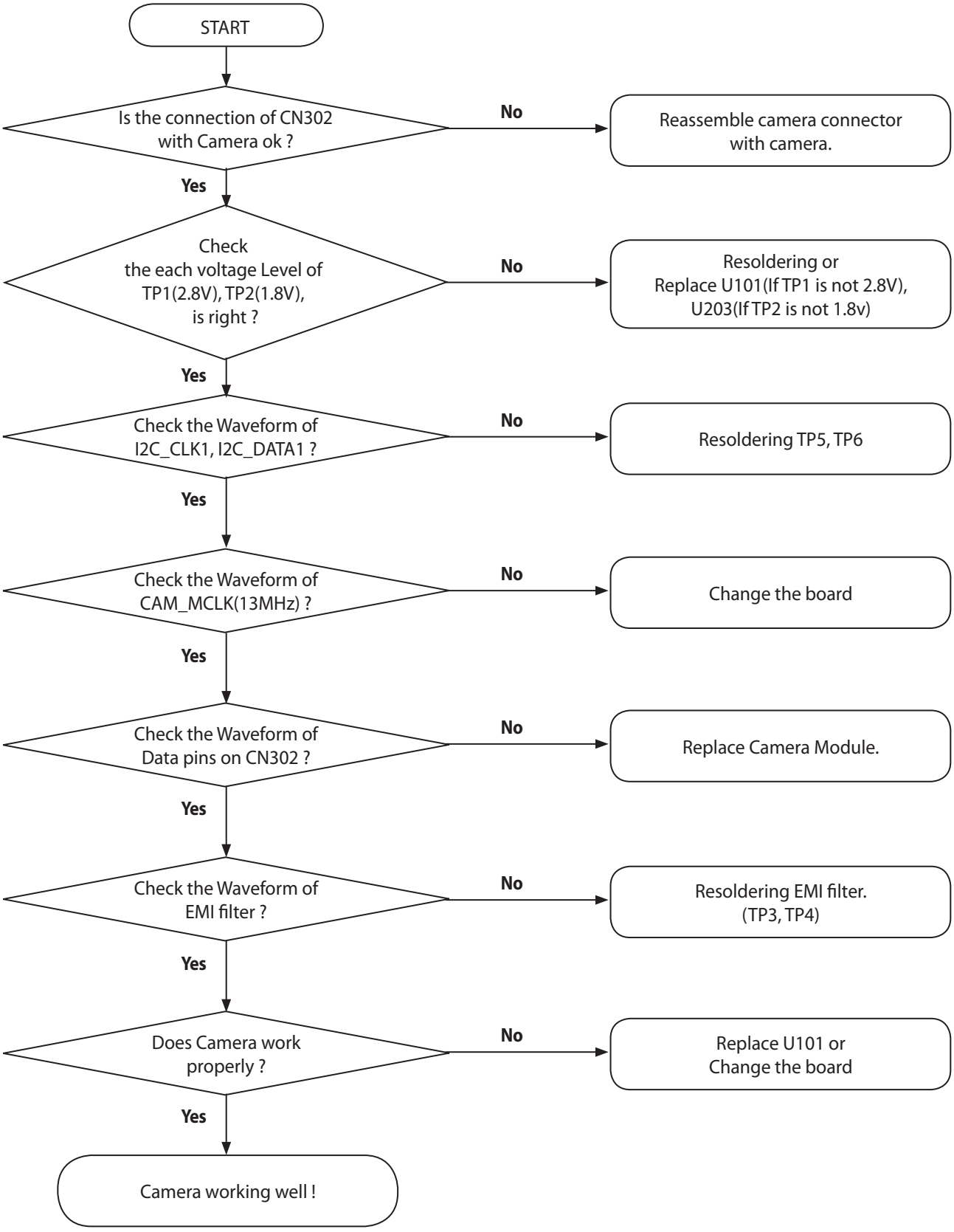
Graph 4.8.2. MCLK Waveform



Graph 4.8.3.CAM_VSYNC vs.
CAM_HSYNC Waveform



Graph 4.8.4.CAM_HSYNC vs.
CAM_PCLK Waveform



4.9 Speaker/ Receiver Trouble

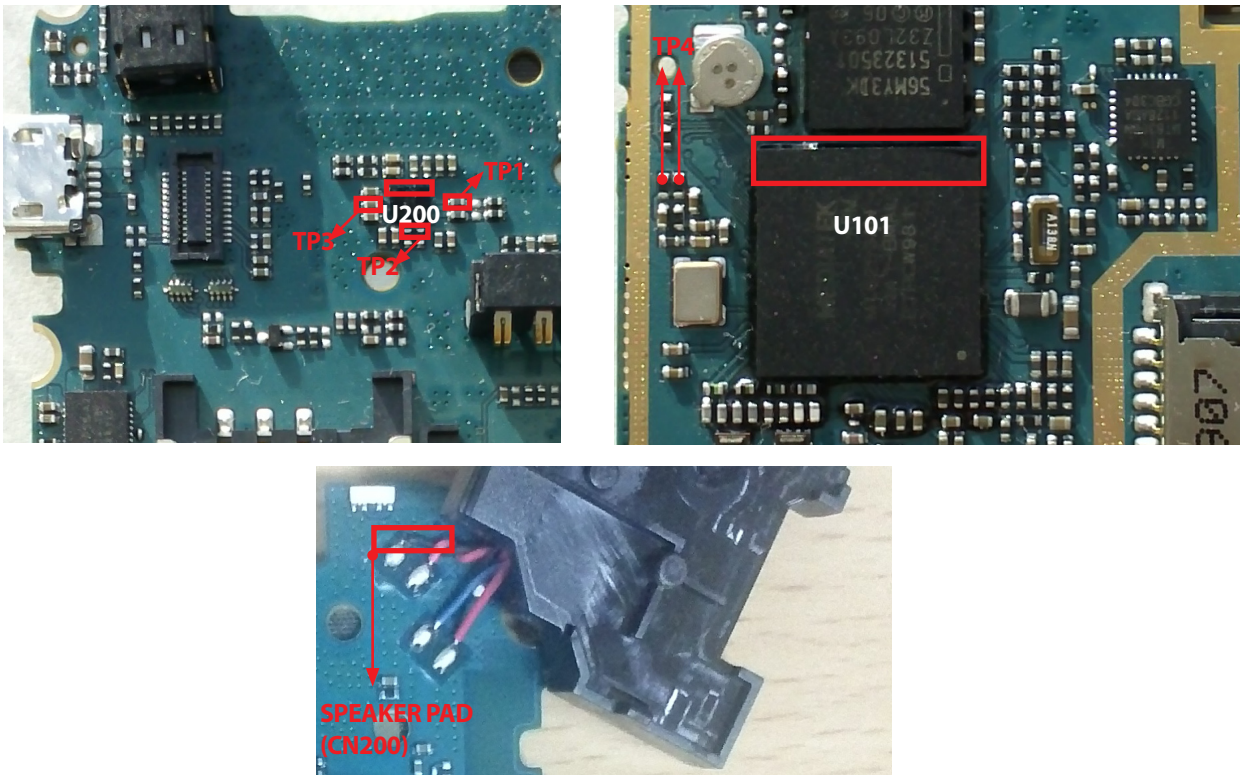
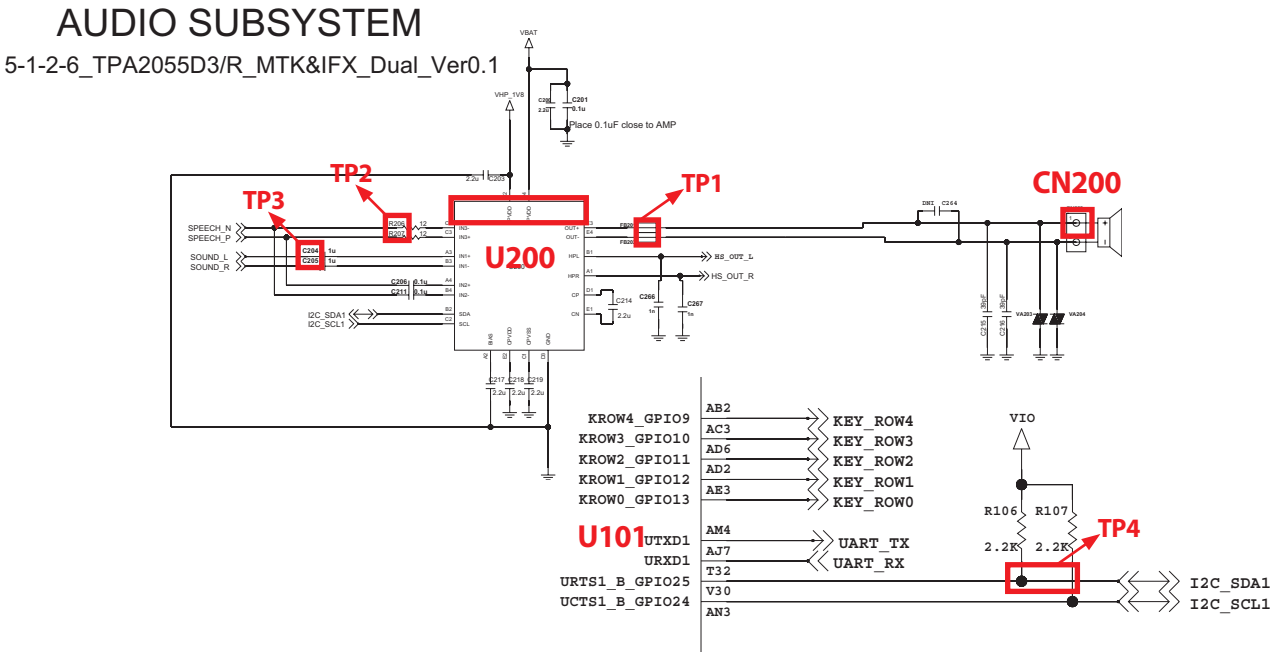
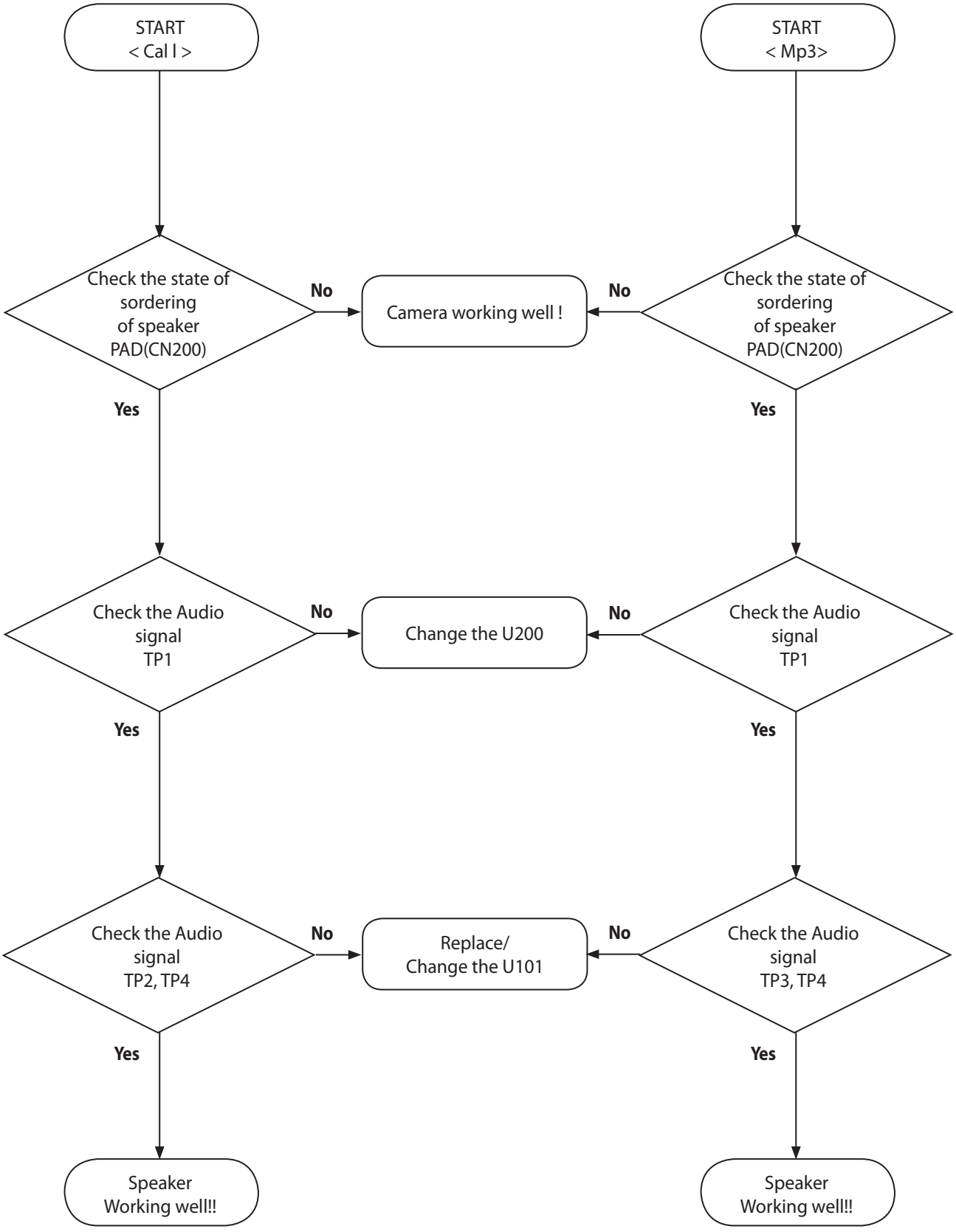


Figure 4.9.1





4.10 3.5φ Headset Trouble

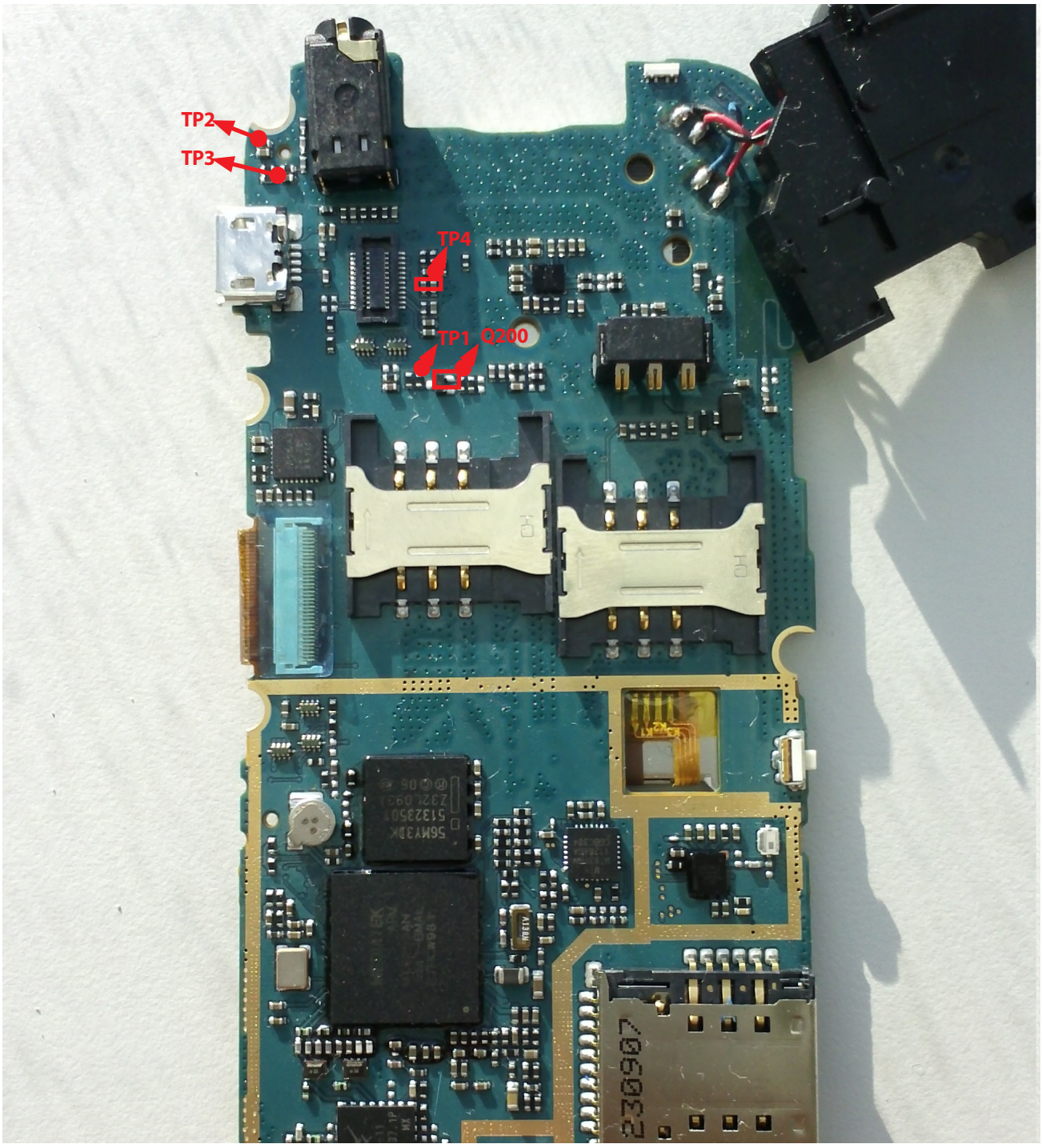


Figure 4.10.1

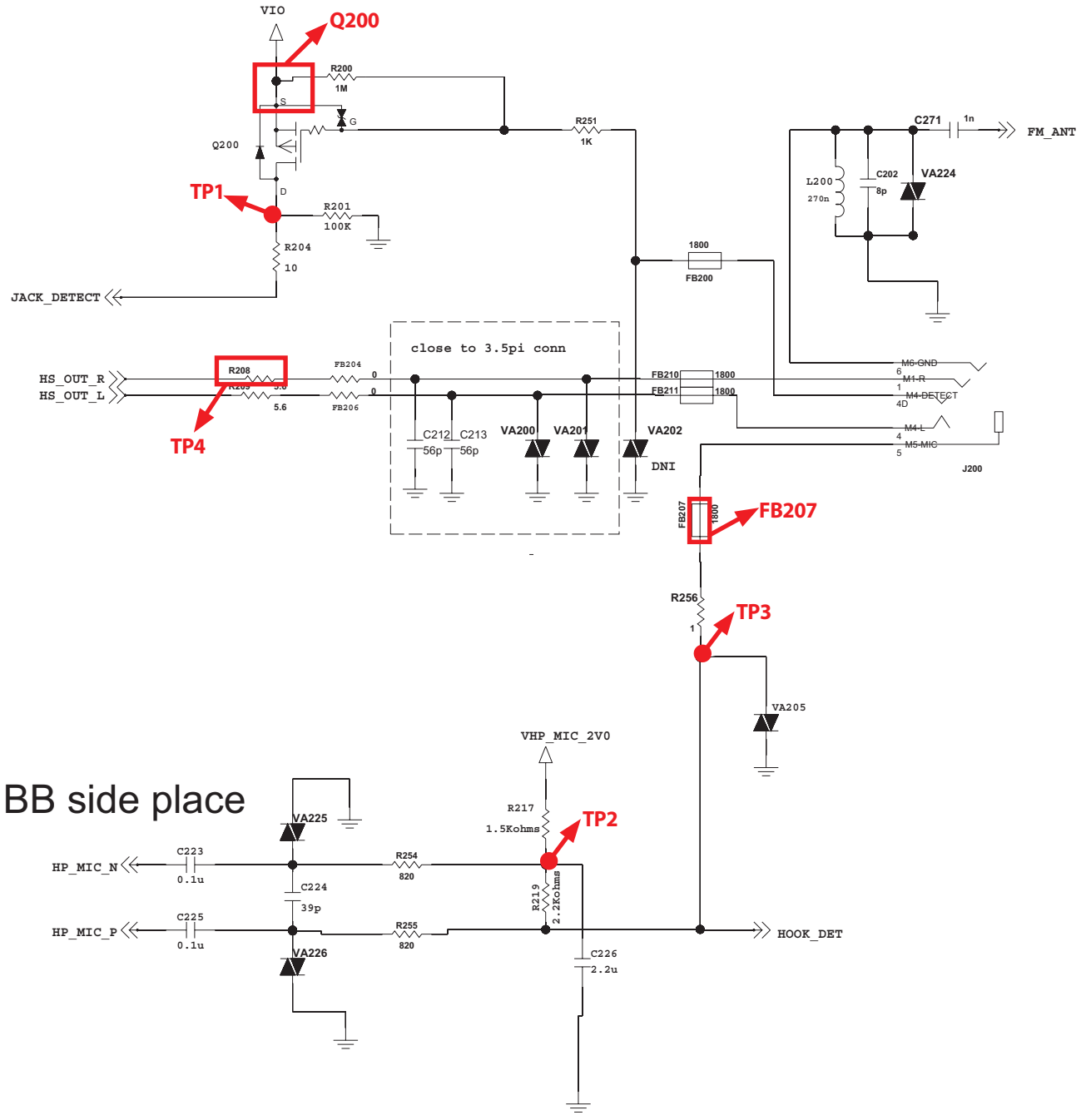
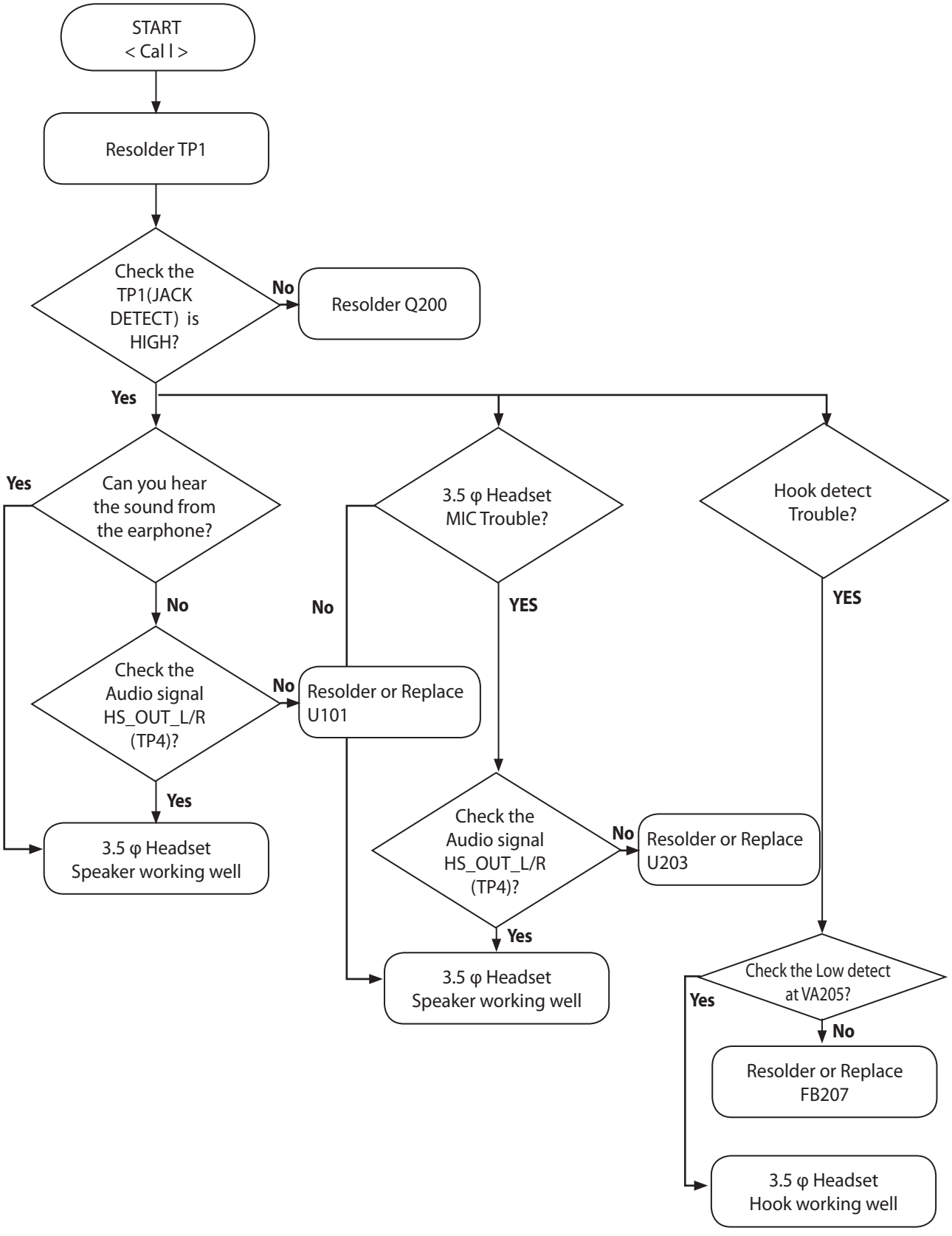


Figure 4.10.1



4.11 Microphone Trouble

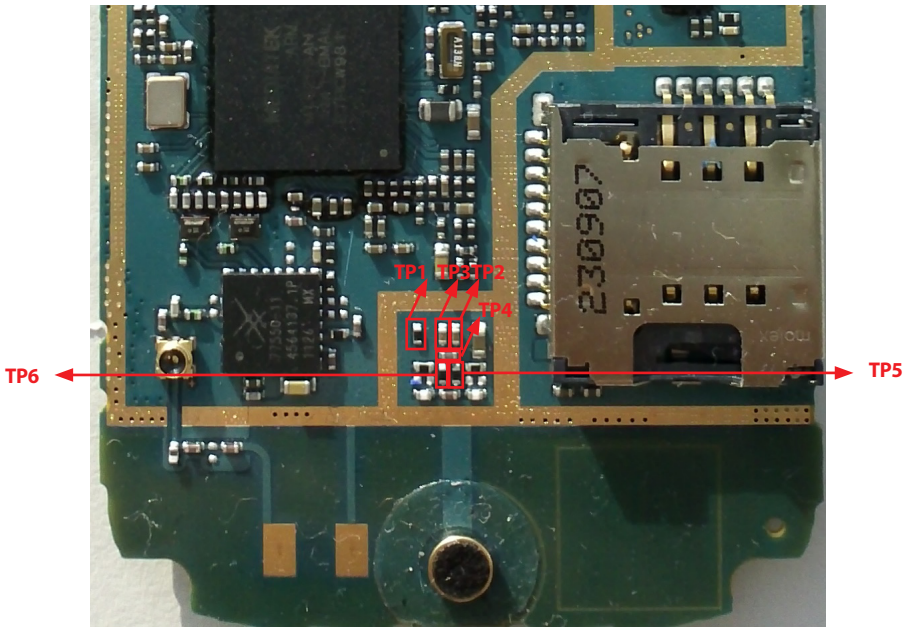
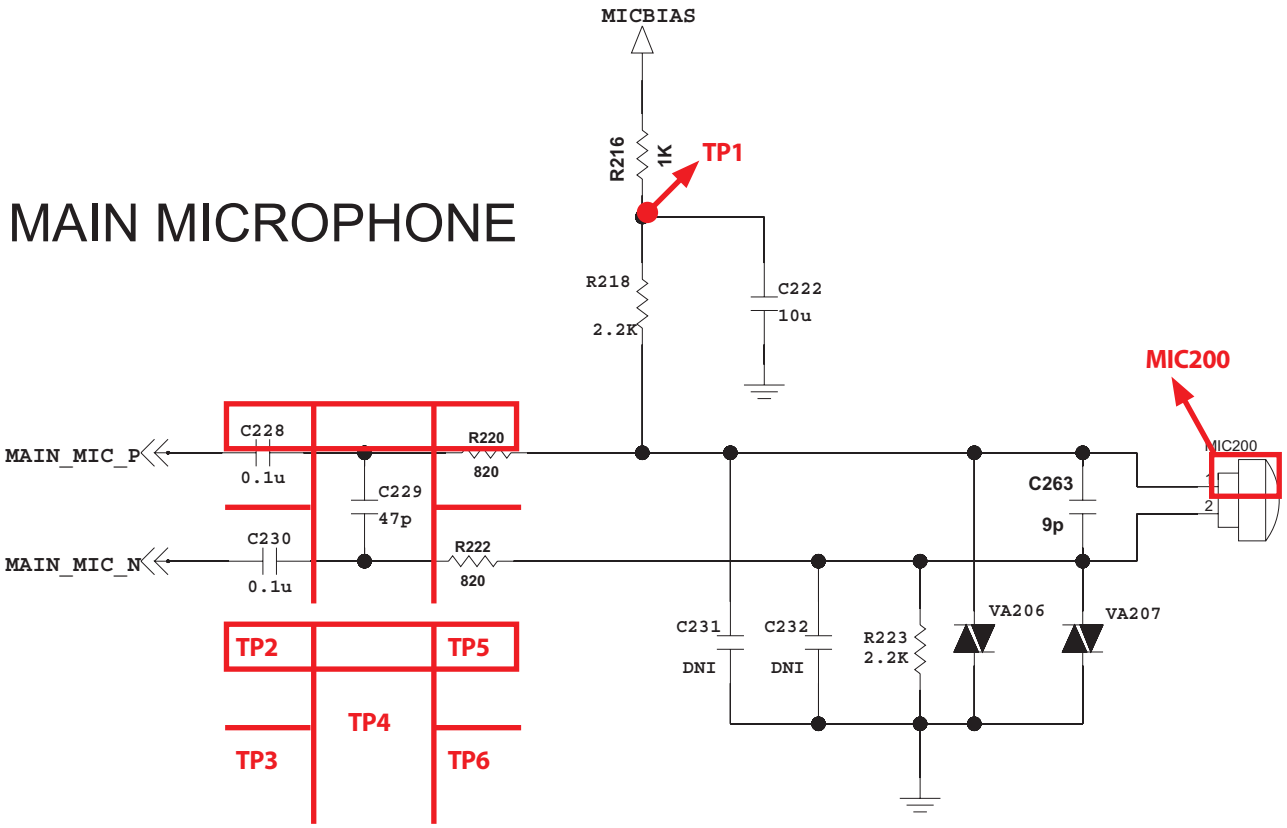
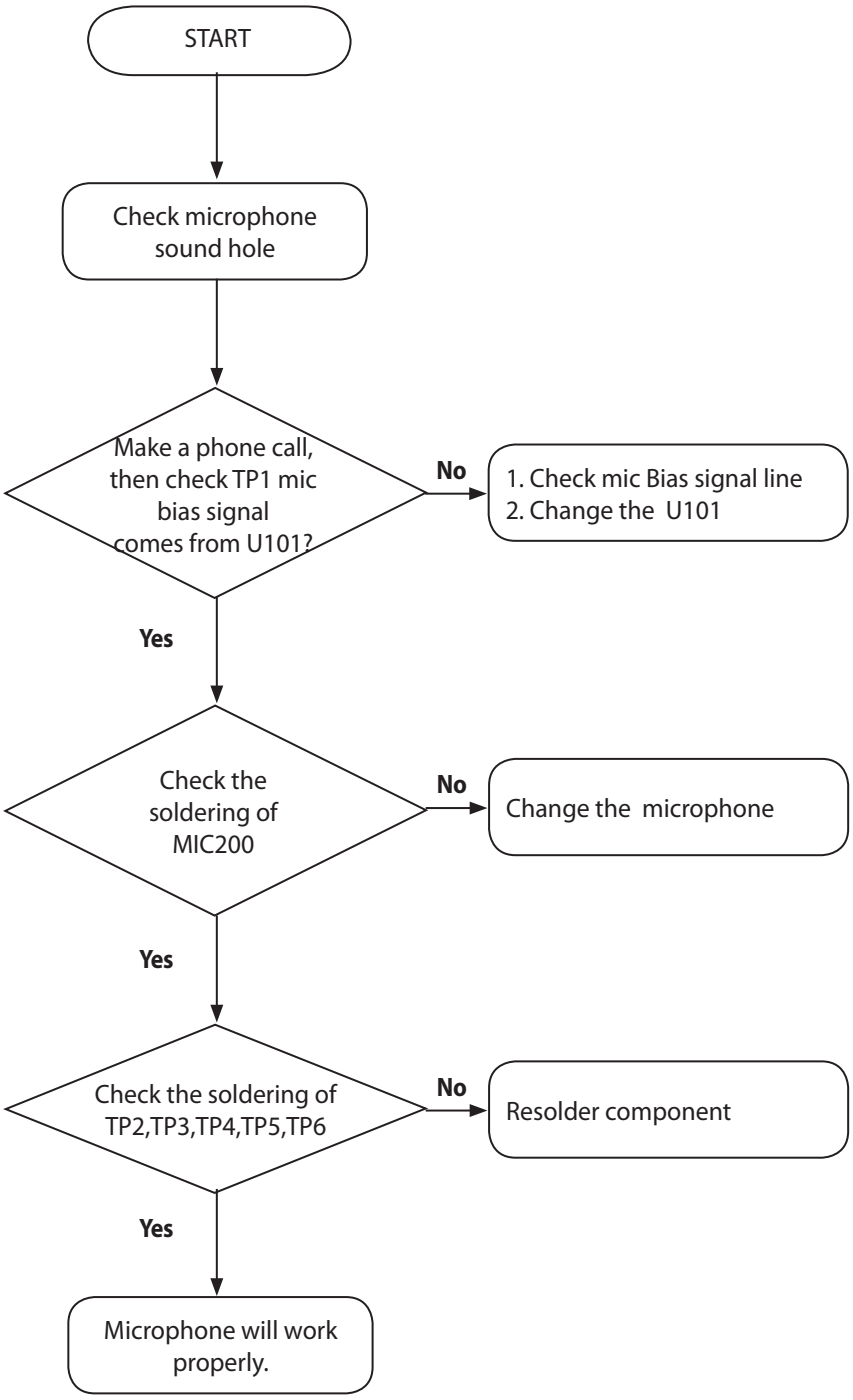


Figure 4.12.1



SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4.12 SIM1 Card Interface Trouble

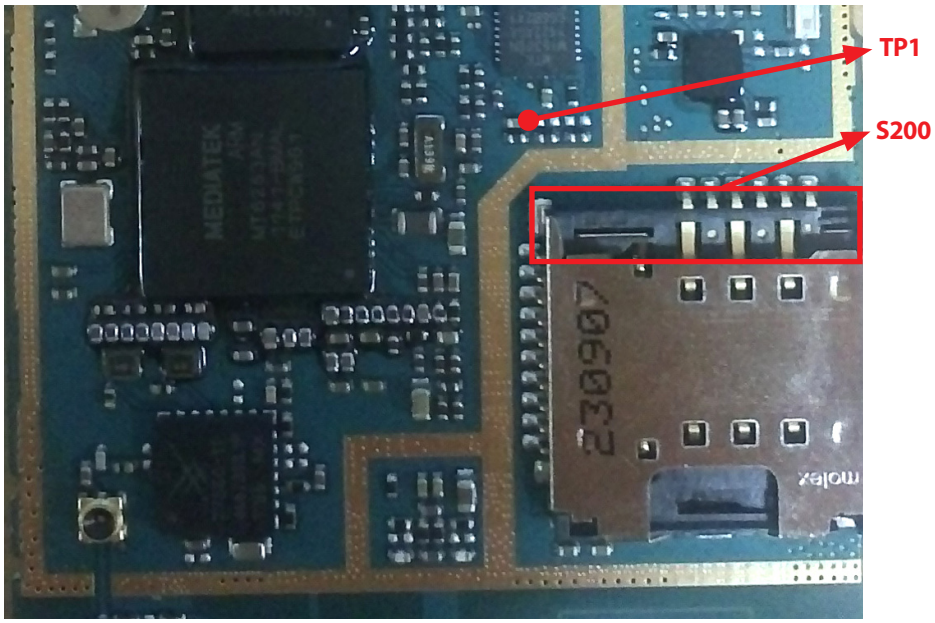


Figure 4.13.1

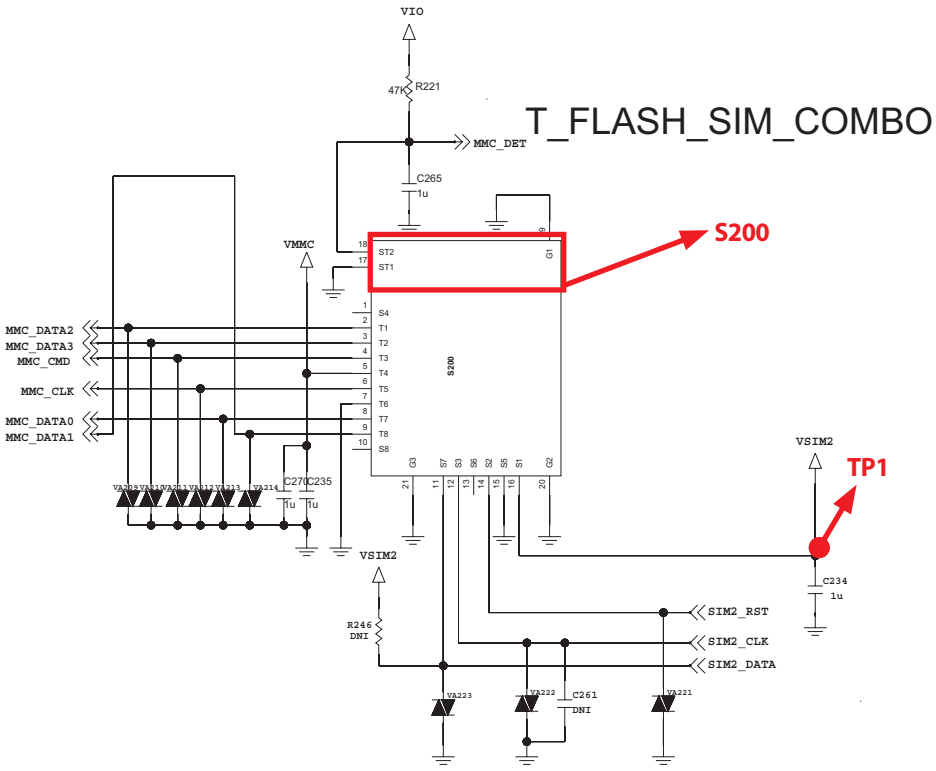
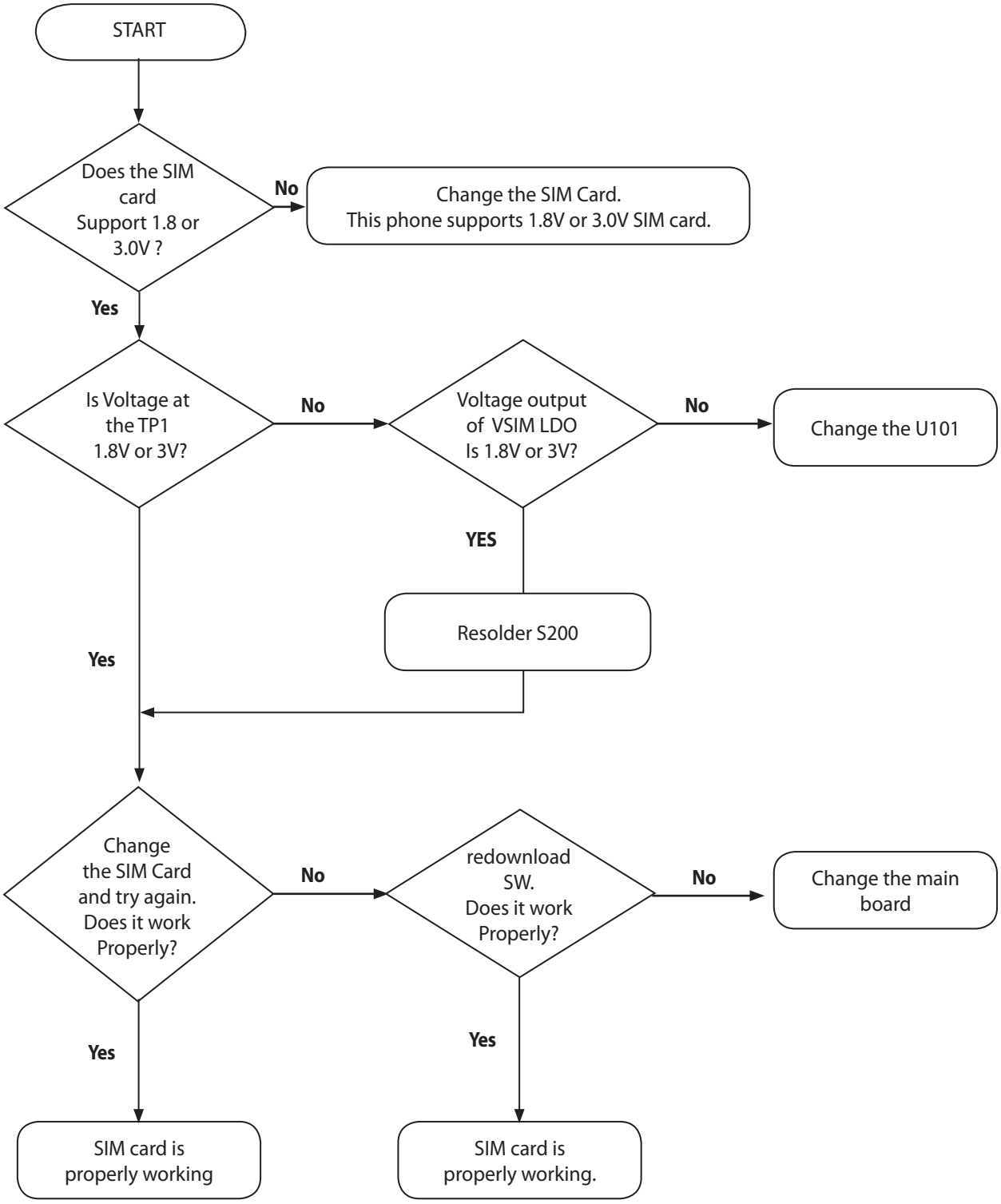


Figure 4.13.1



4.13 SIM2 Card Interface Trouble

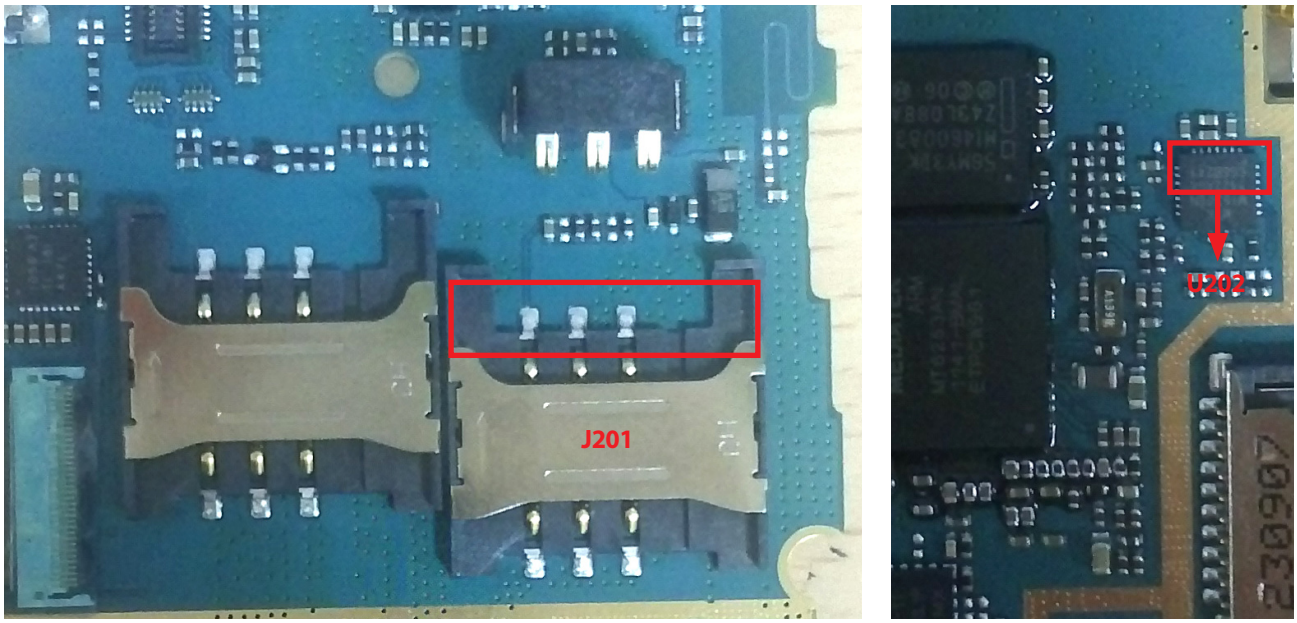
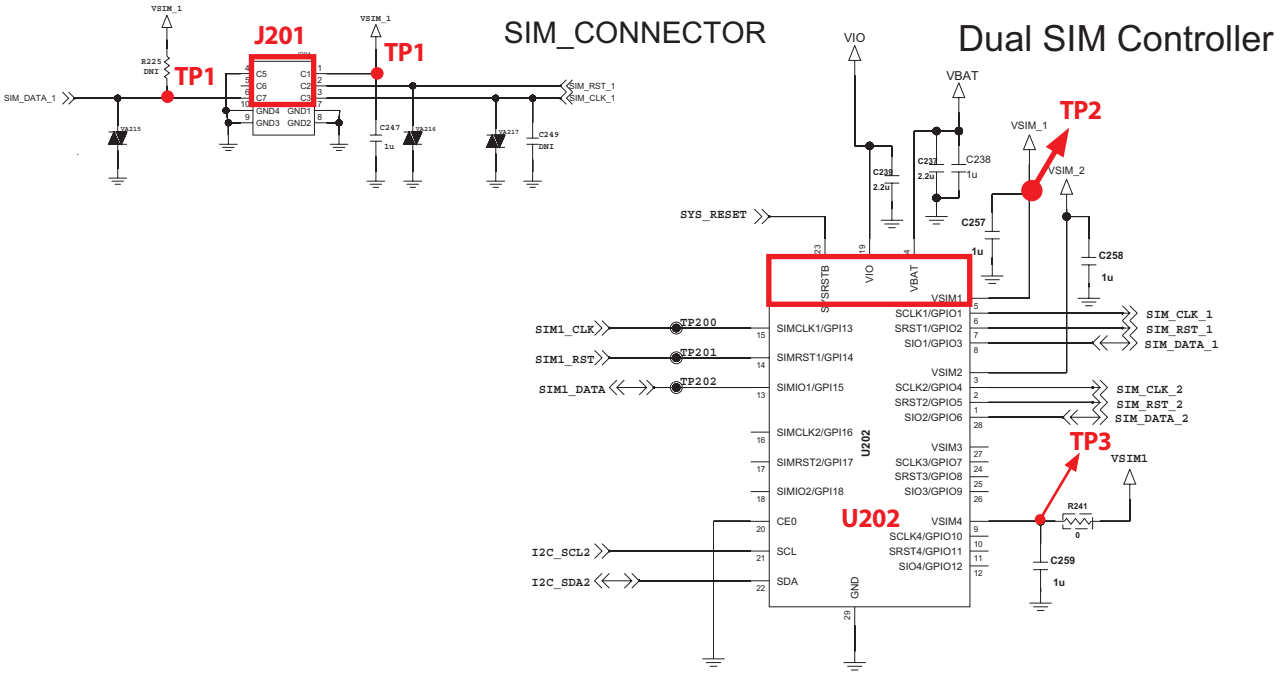
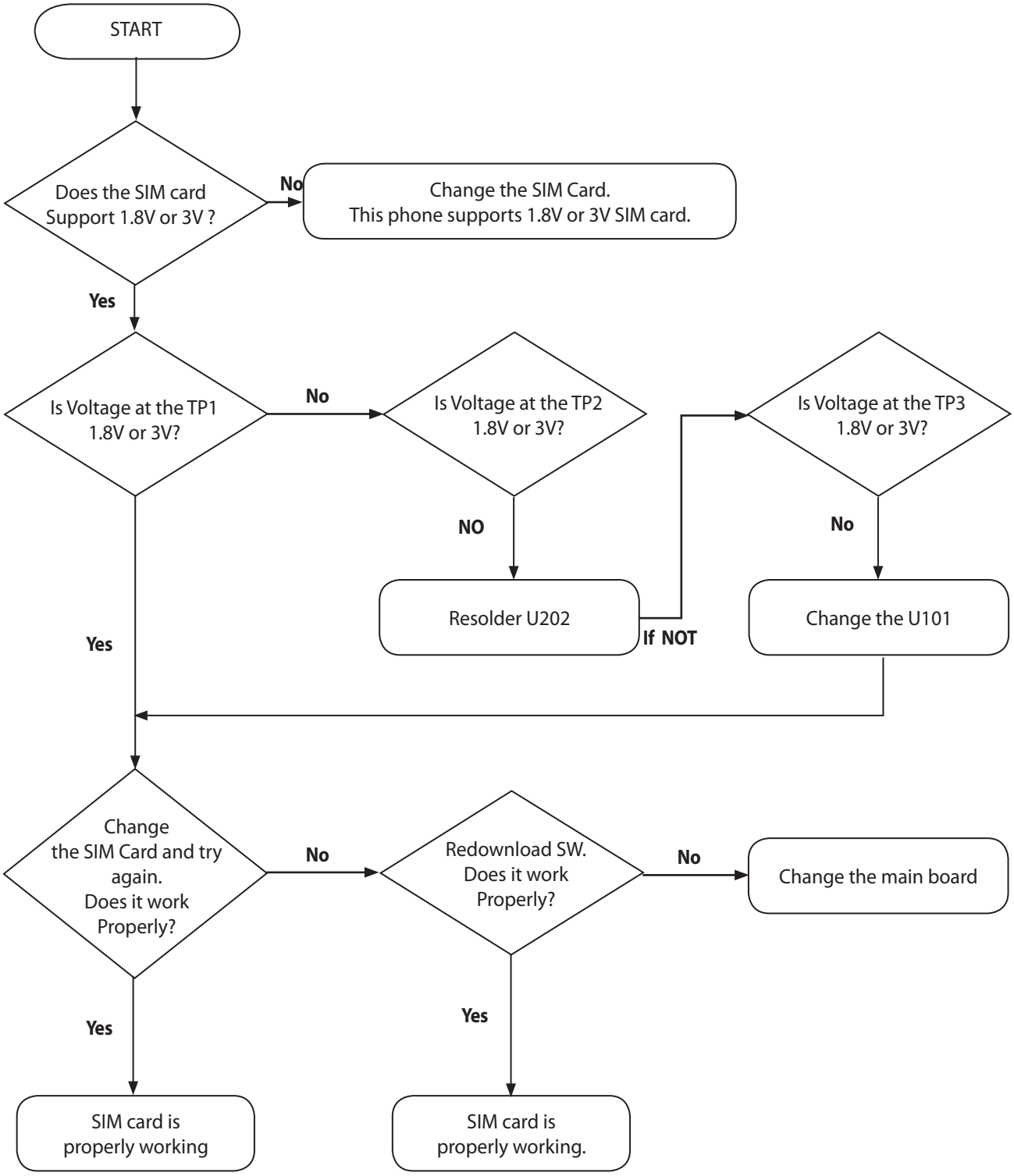


Figure 4.13.1





4.14 SIM3 Card Interface Trouble

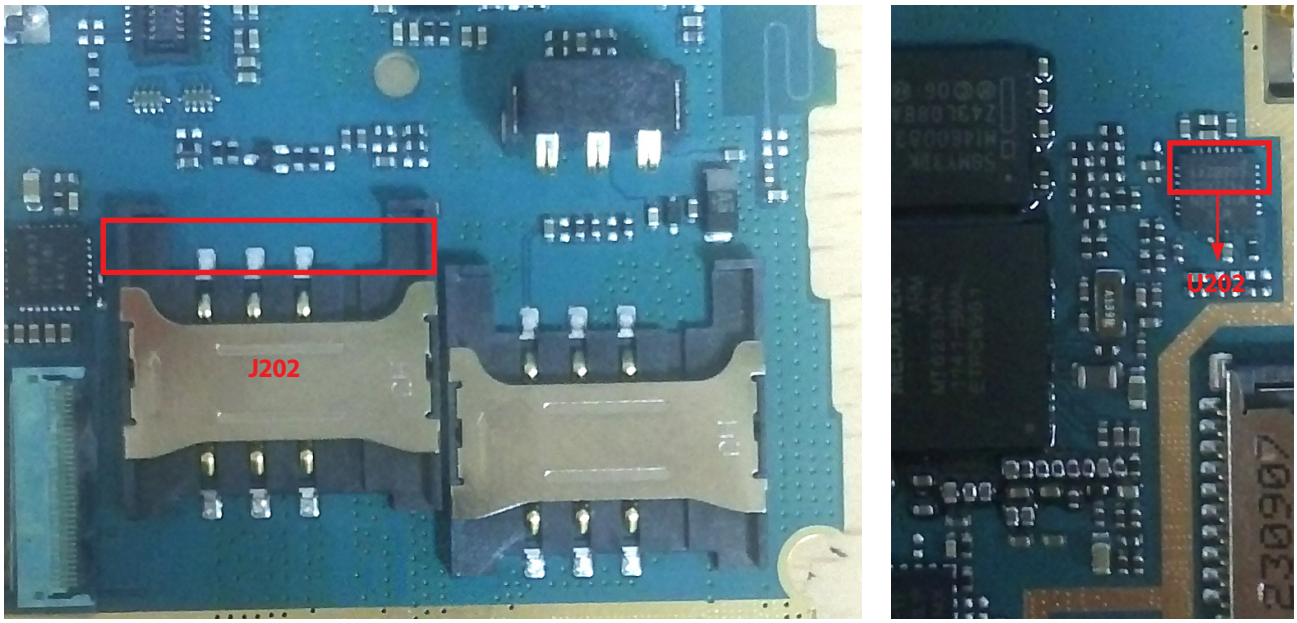
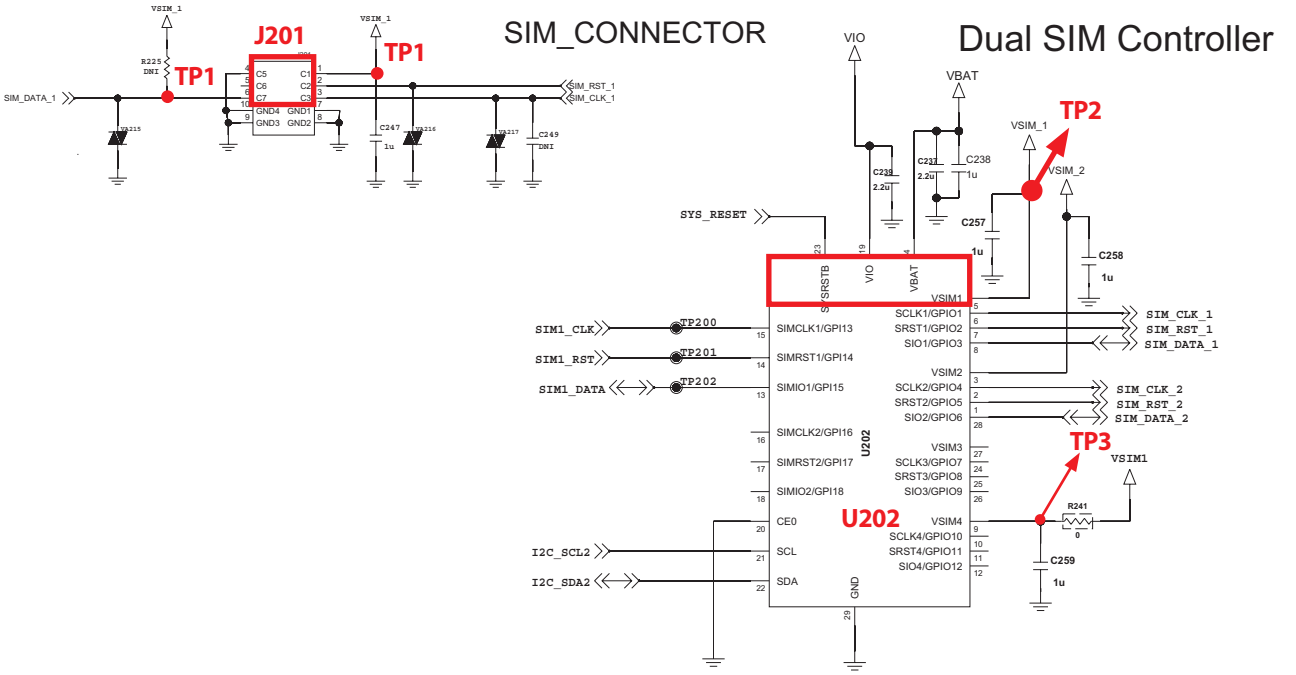
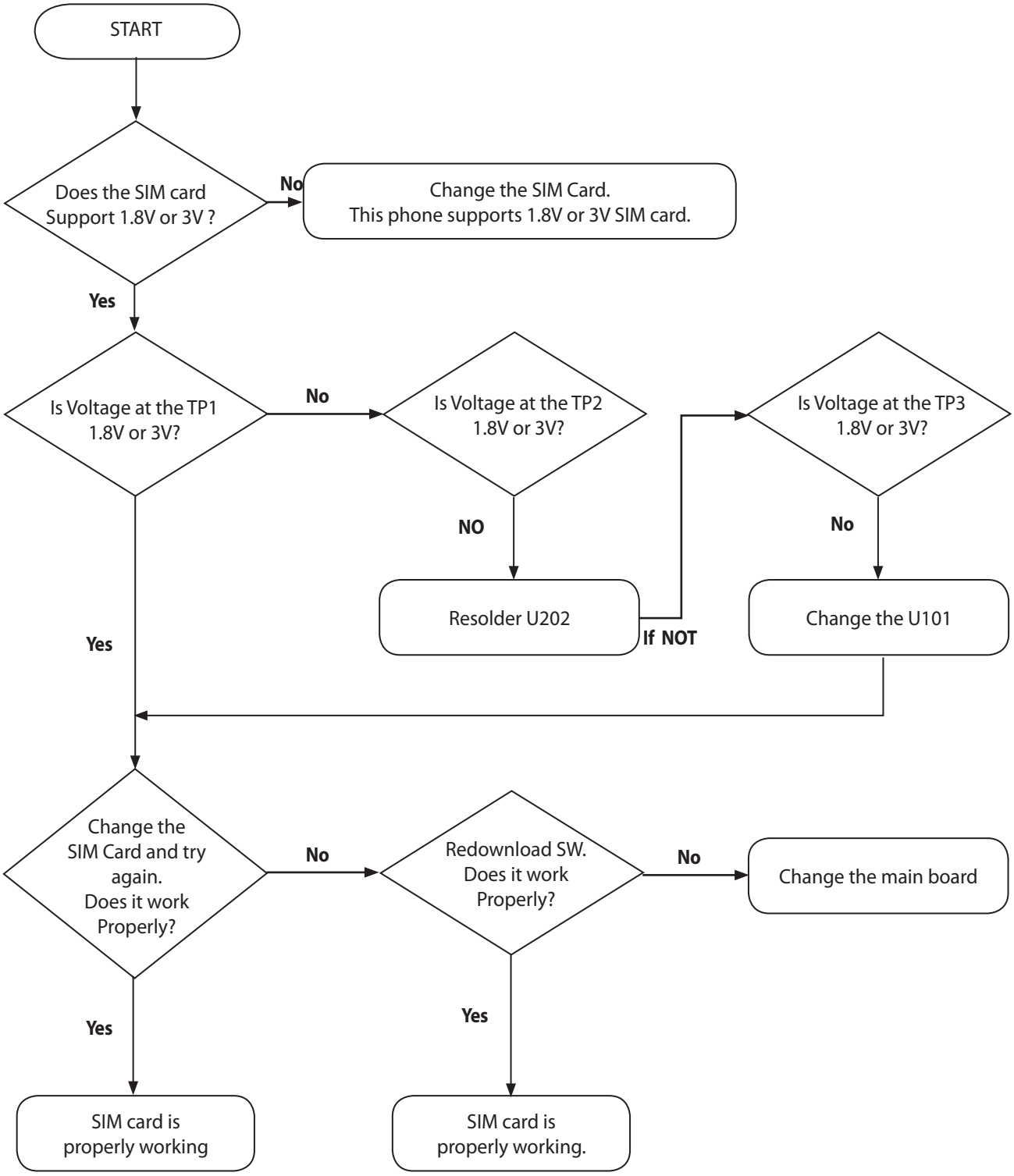


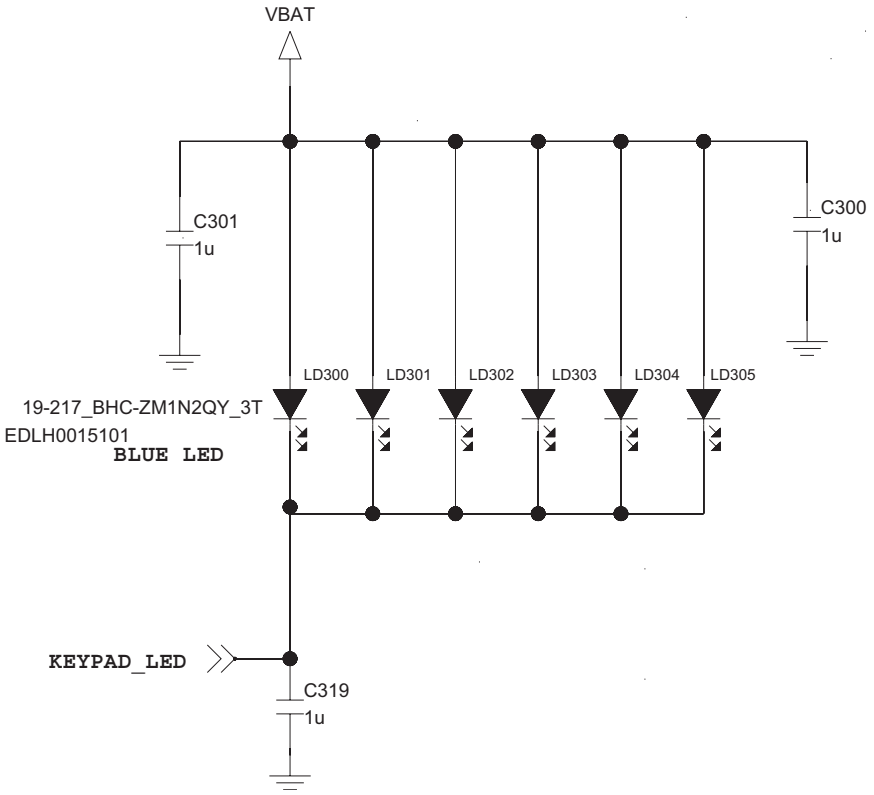
Figure 4.13.1

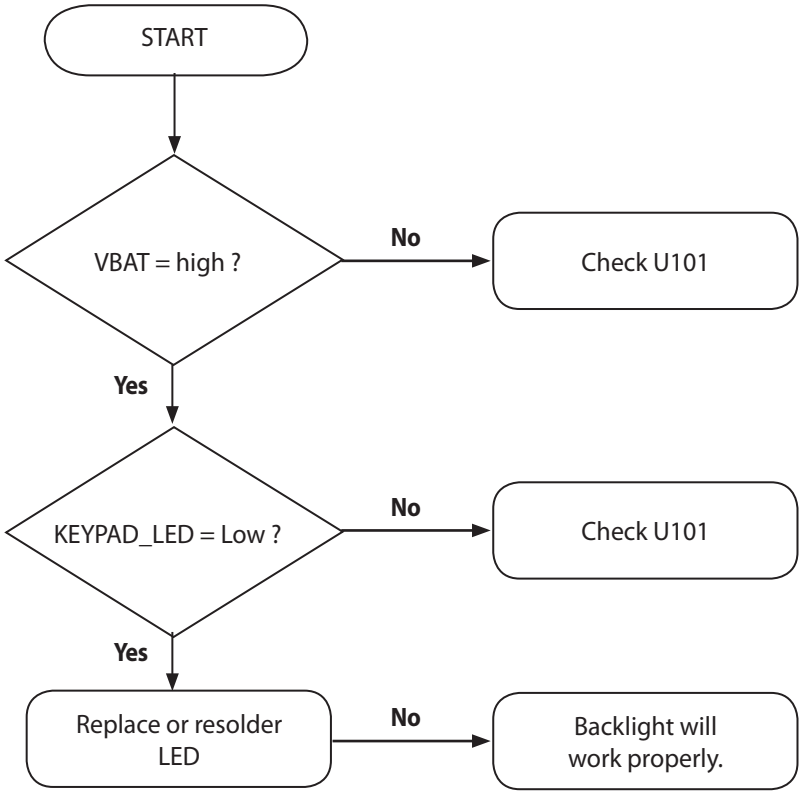




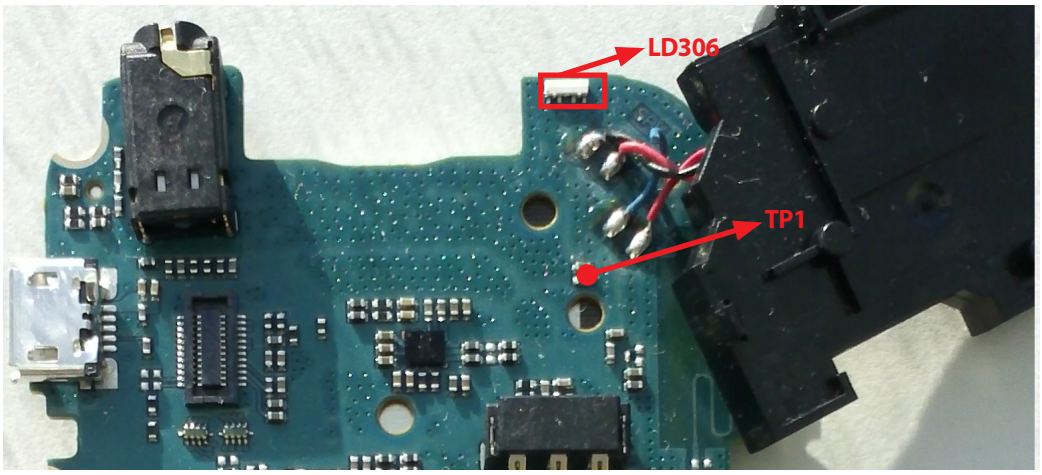
4.15 KEY backlight Trouble

Figure 4.14.1





4.16 Torch Trouble



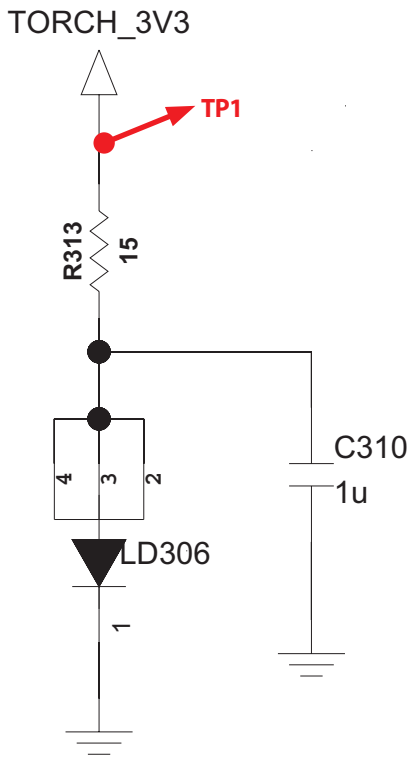
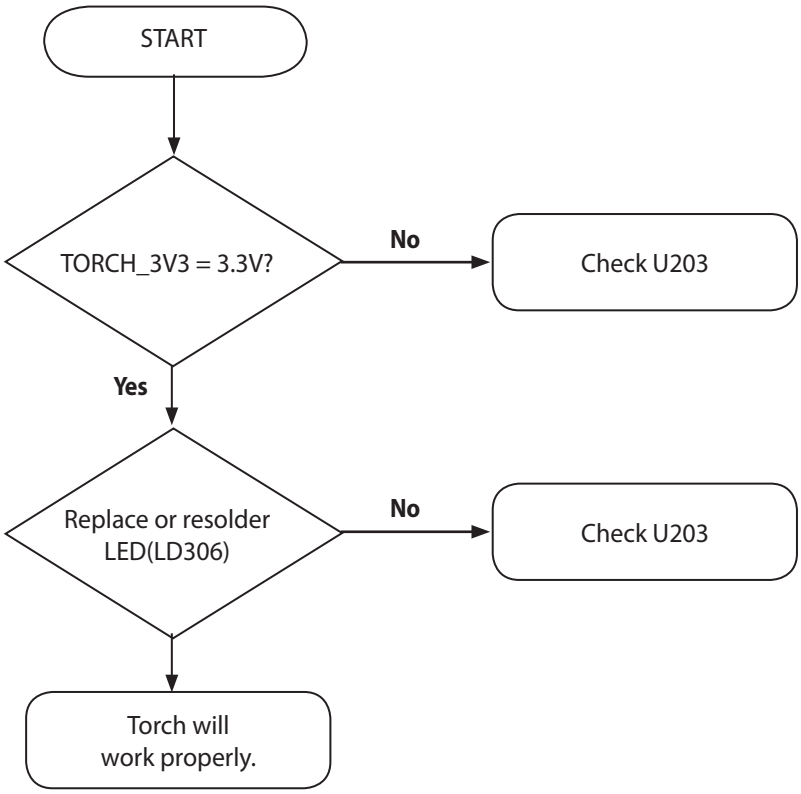
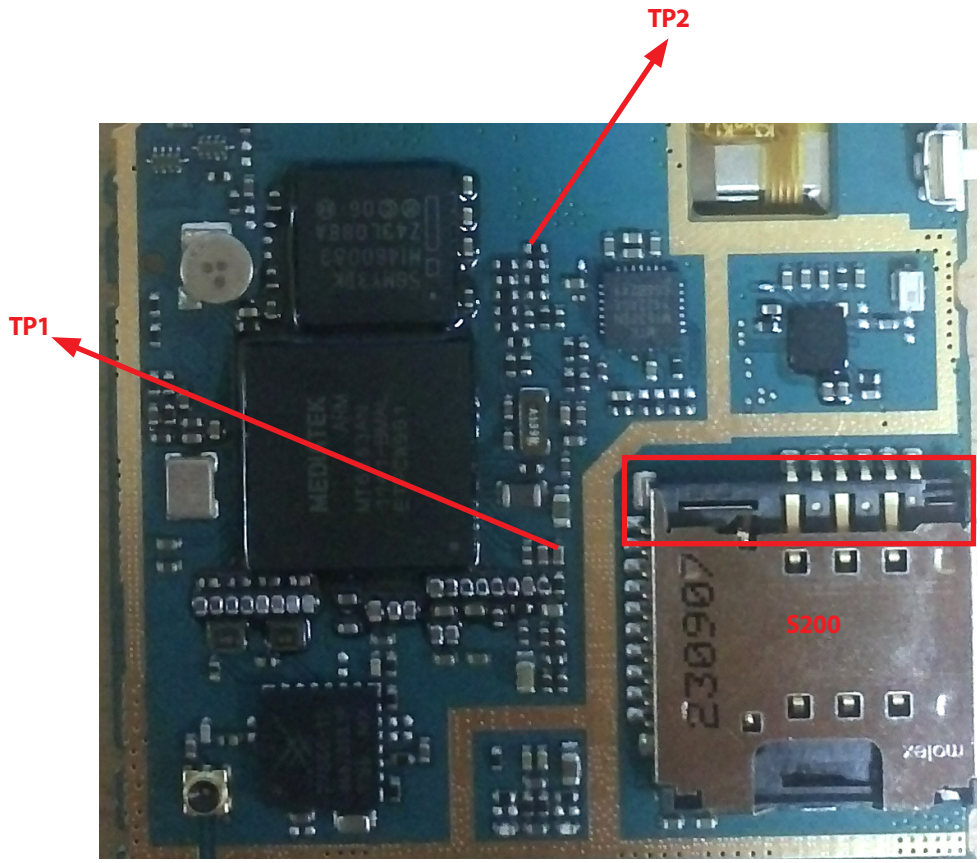
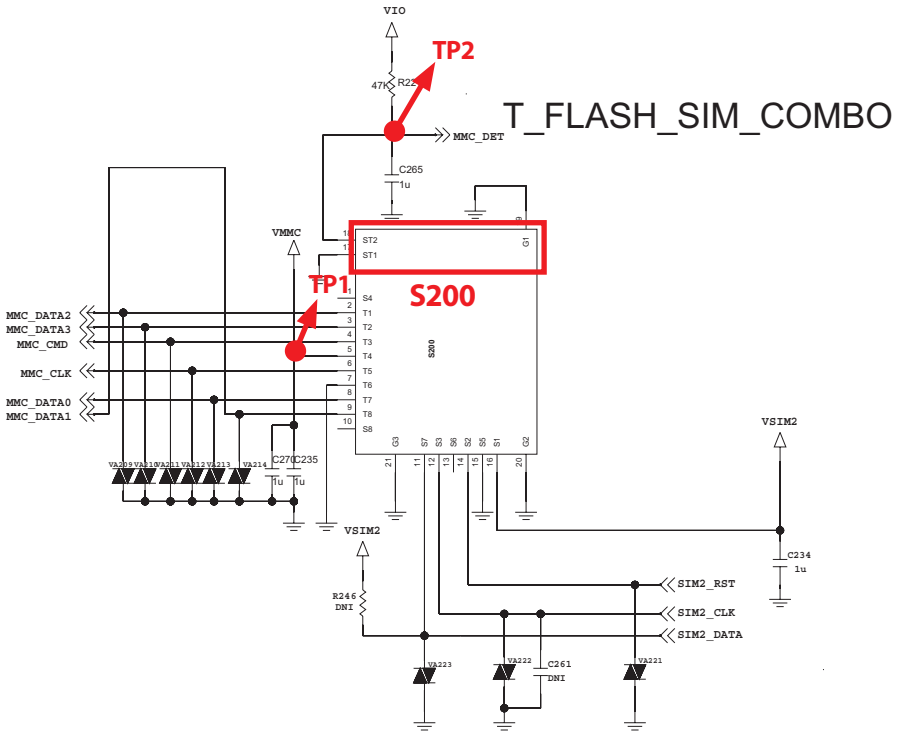


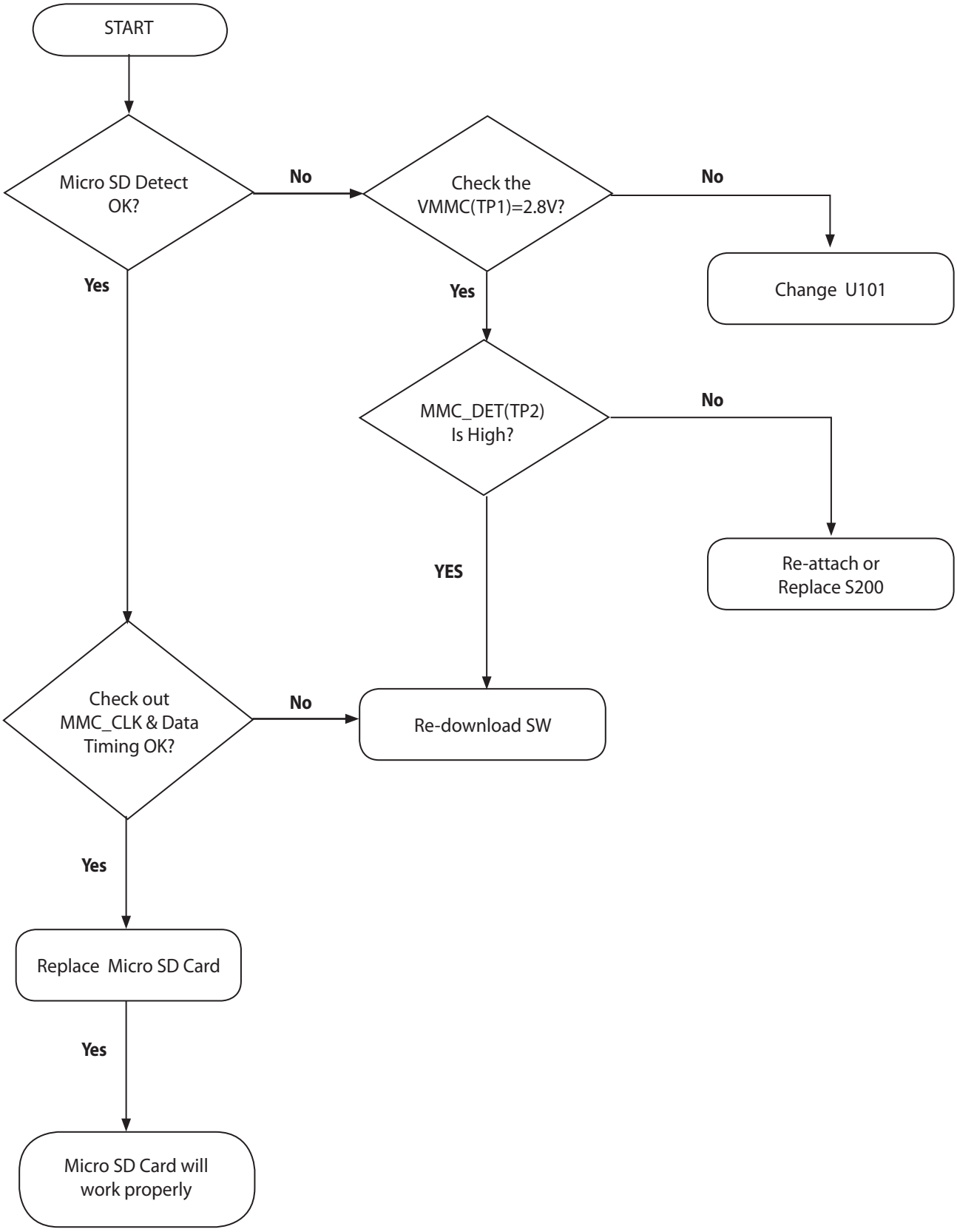
Figure 4.14.1



4.17 Micro SD Trouble







4.18 Bluetooth Trouble

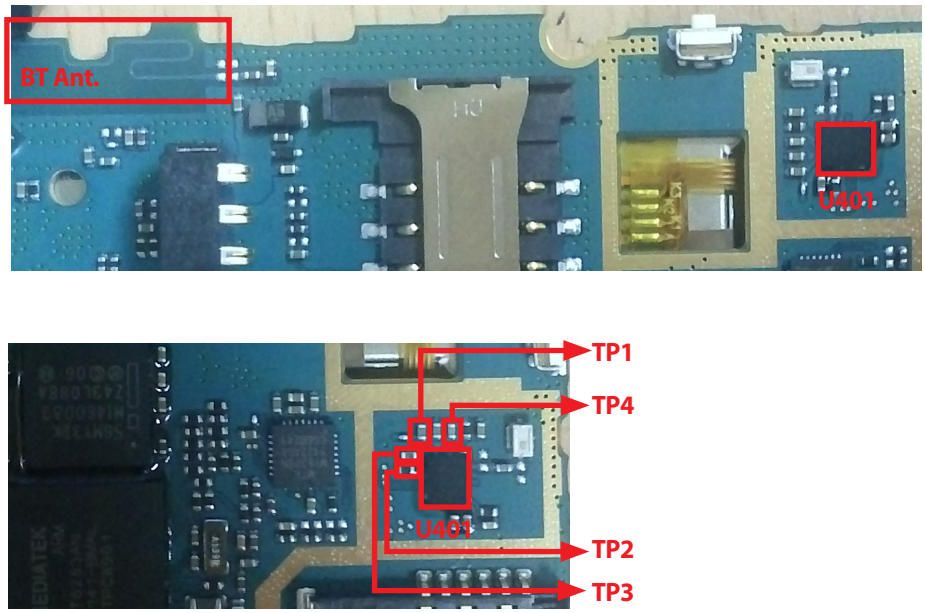
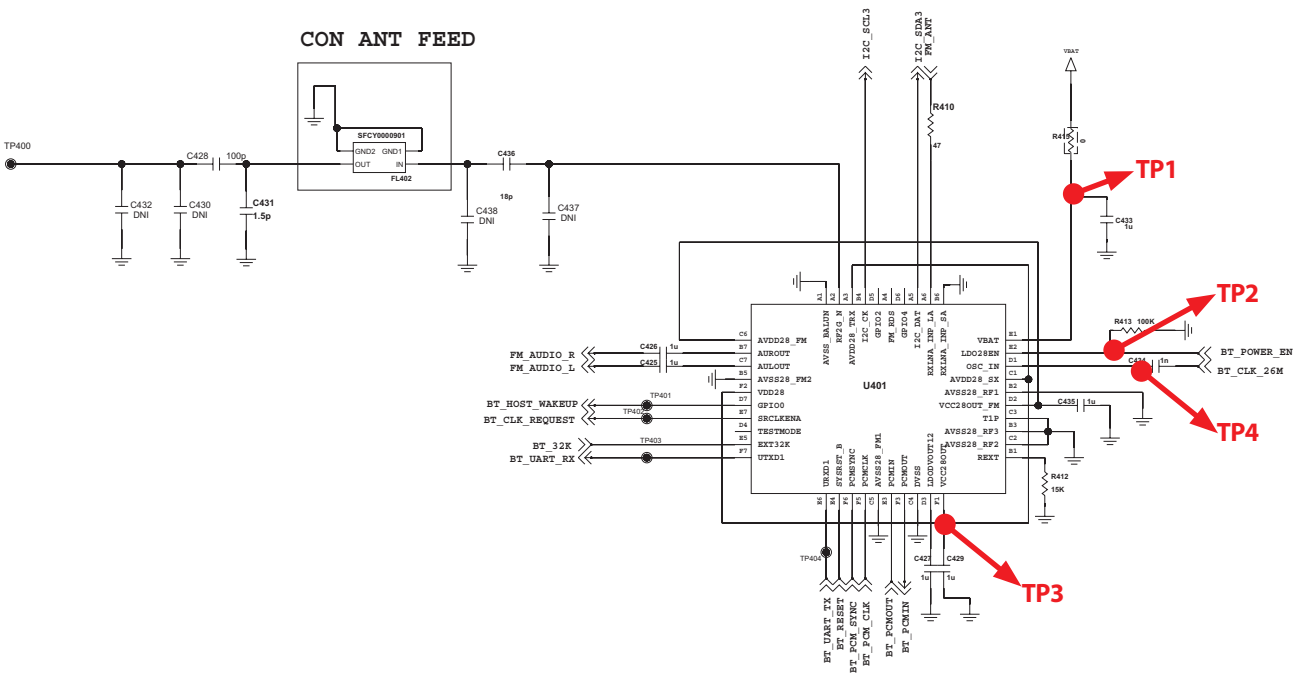
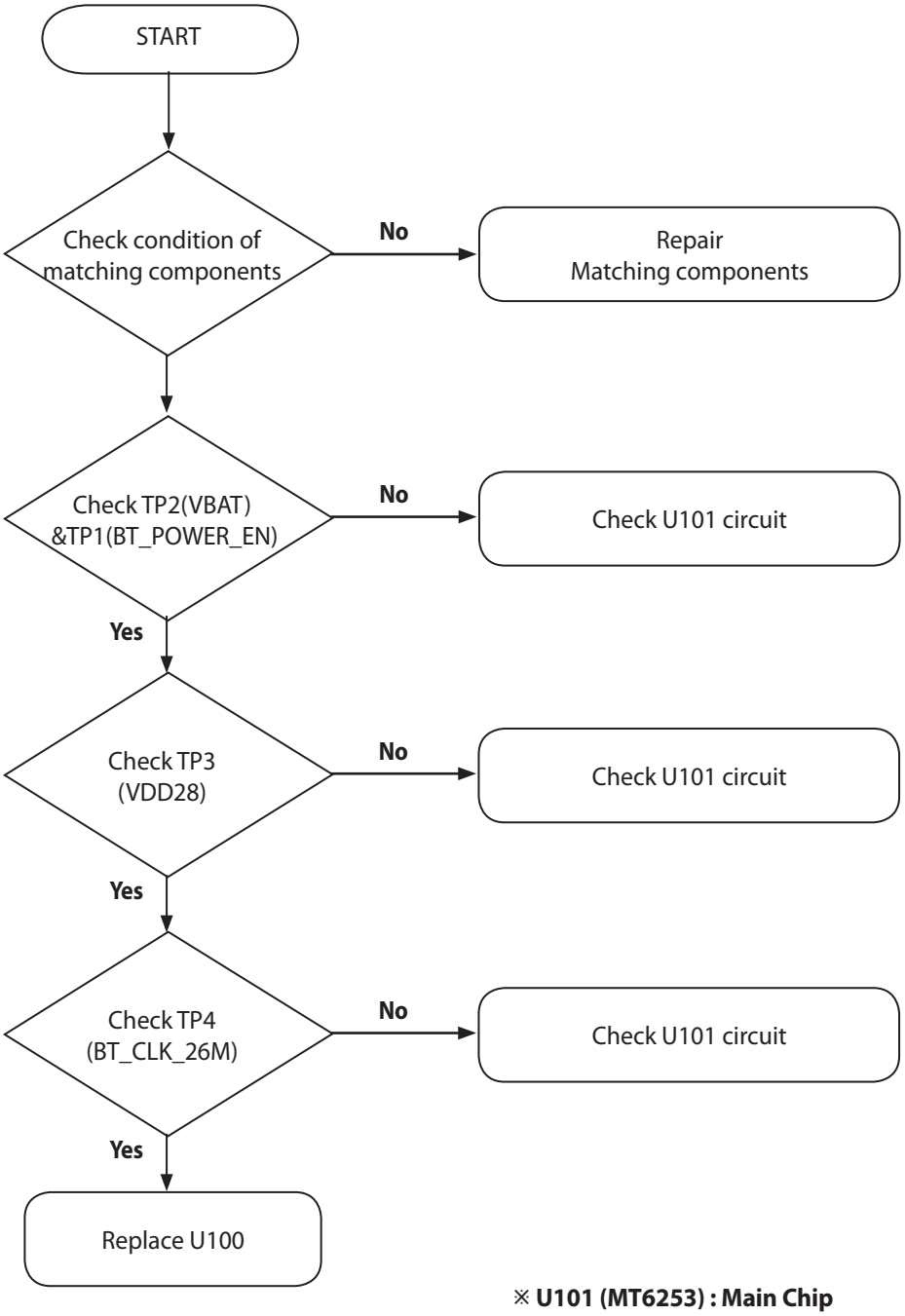


Figure 4.15.1





※ **U101 (MT6253) : Main Chip**

4.19 FM Radio Trouble

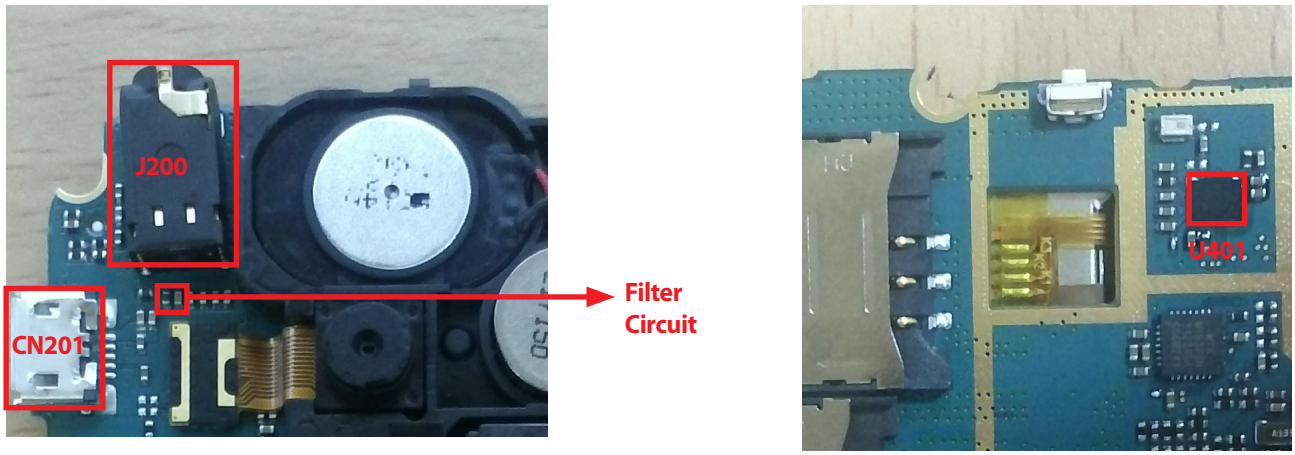
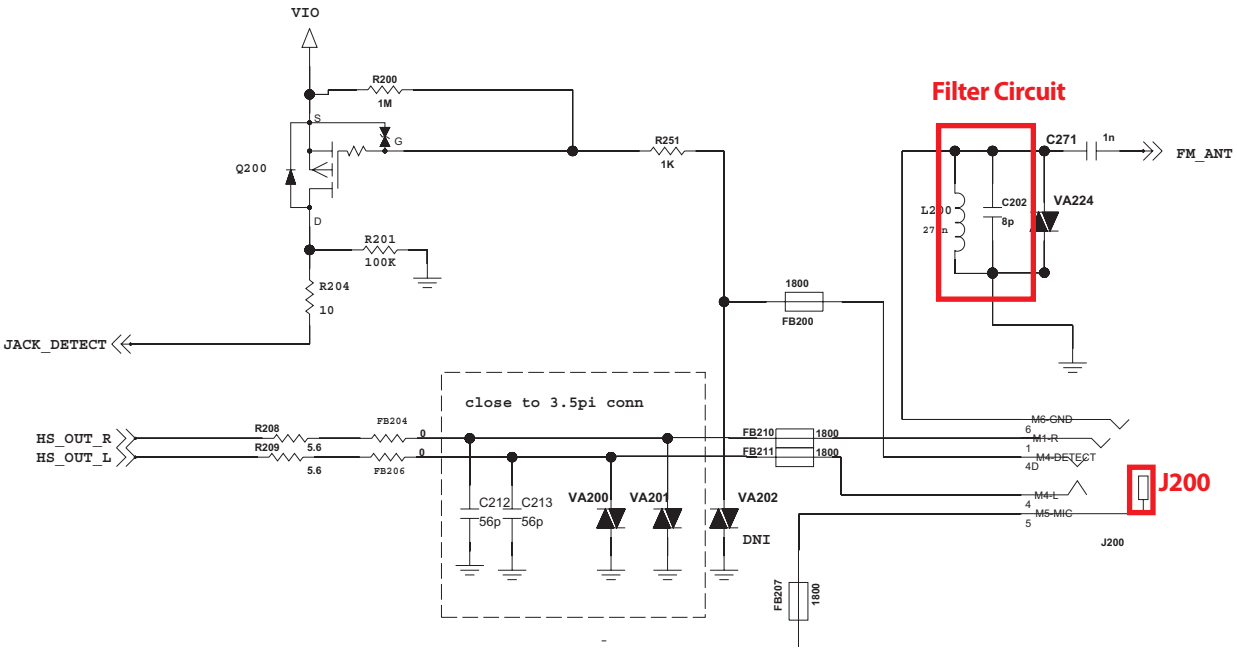
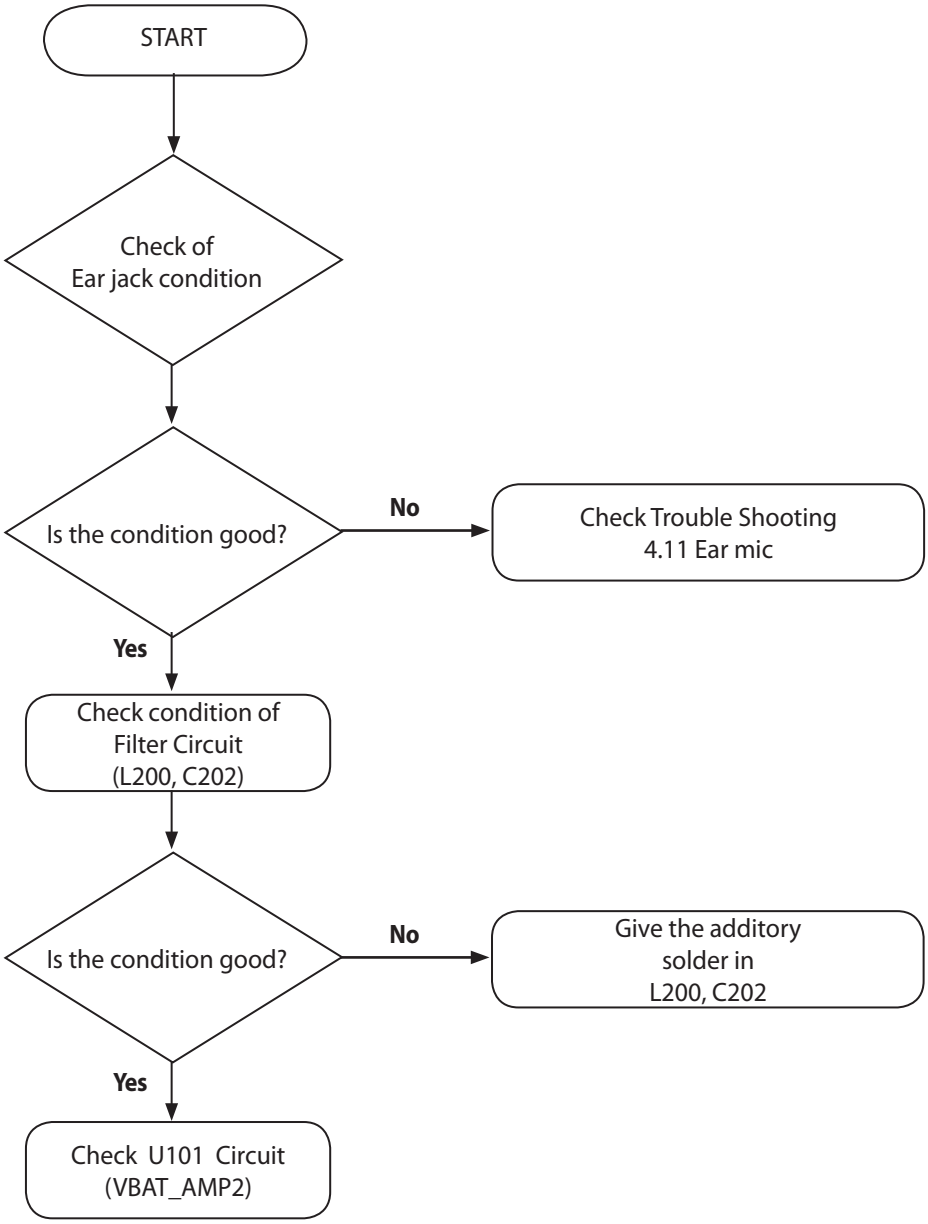
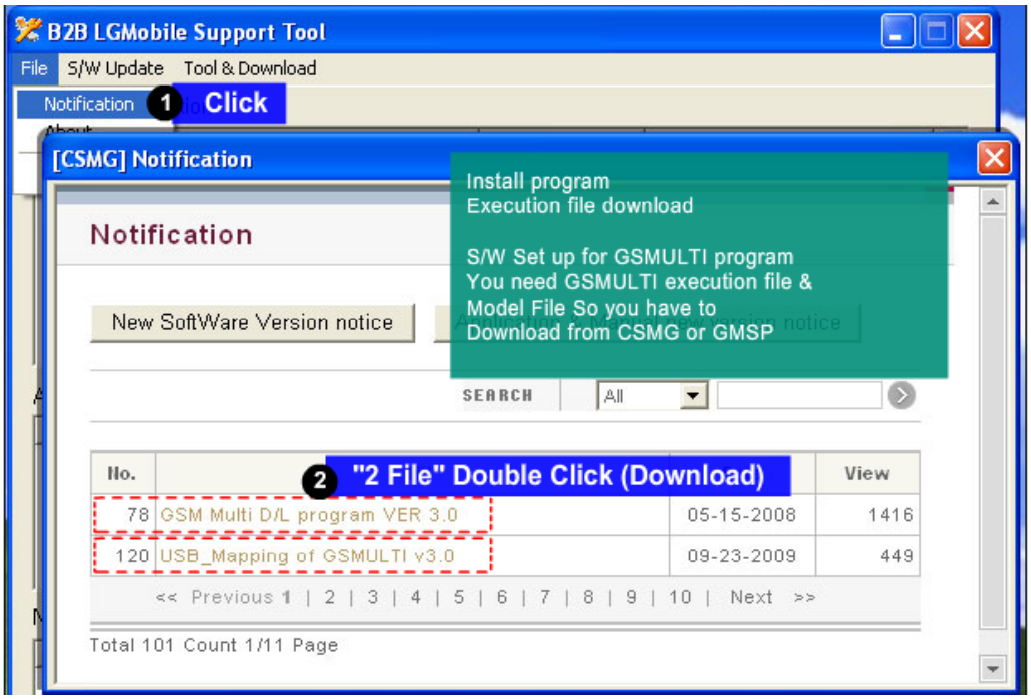


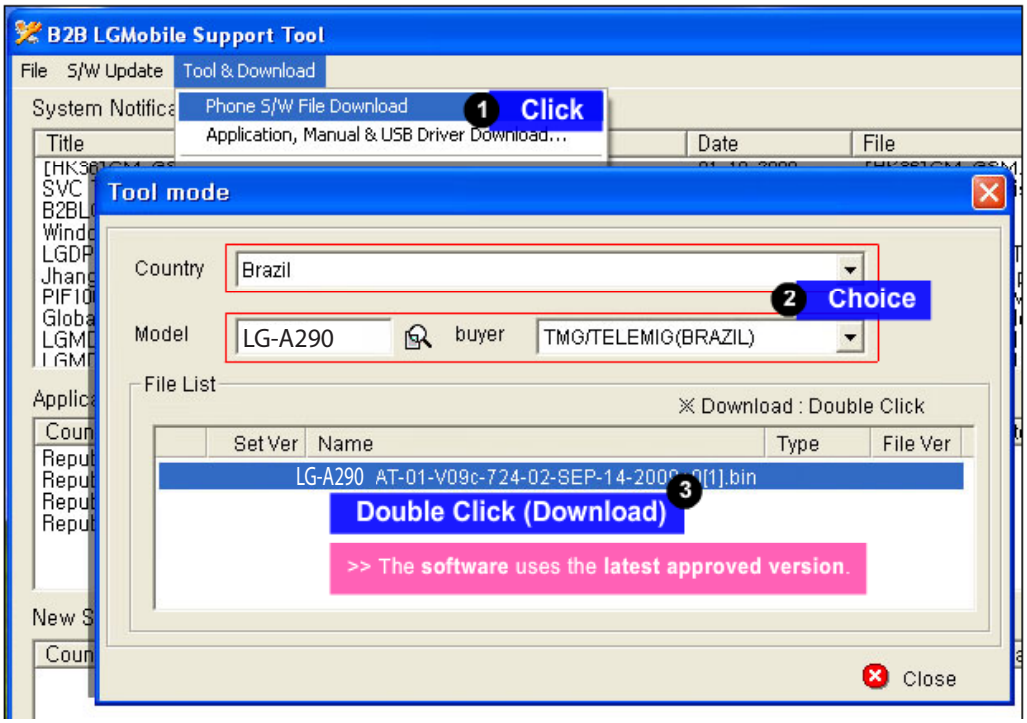
Figure 4.17.1

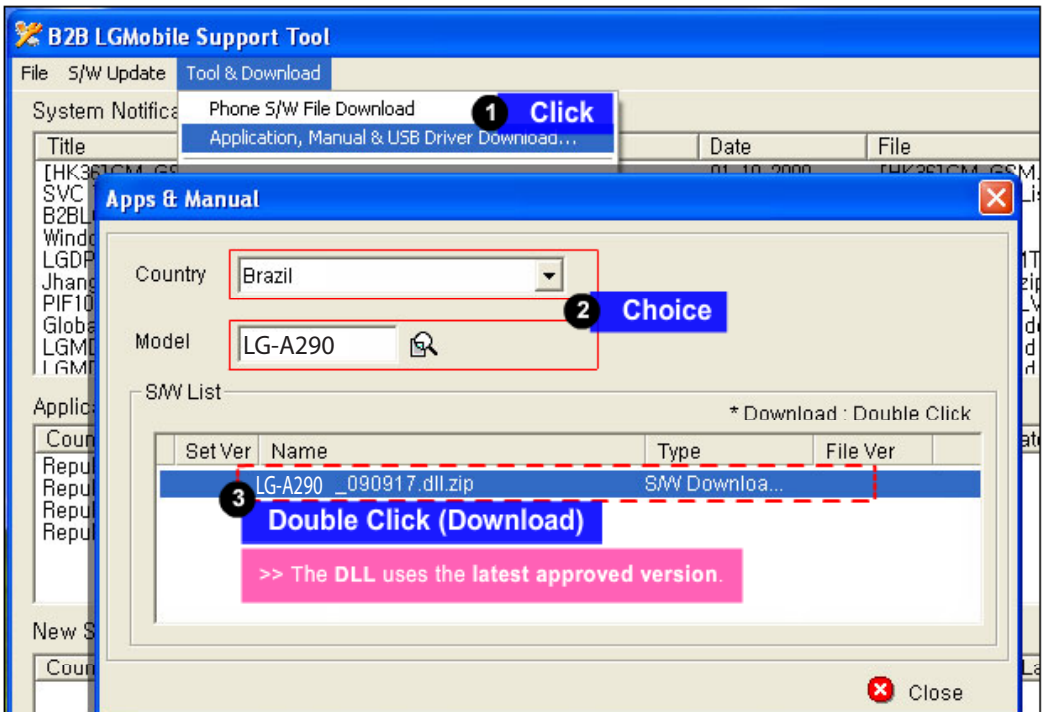


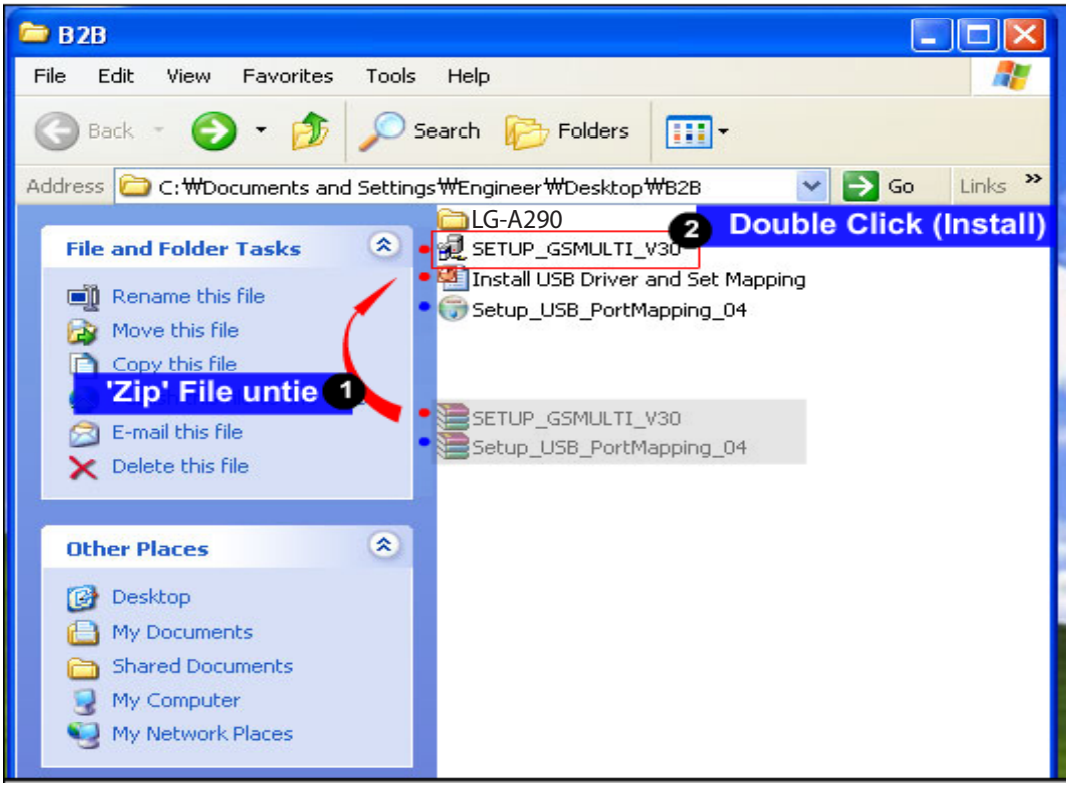


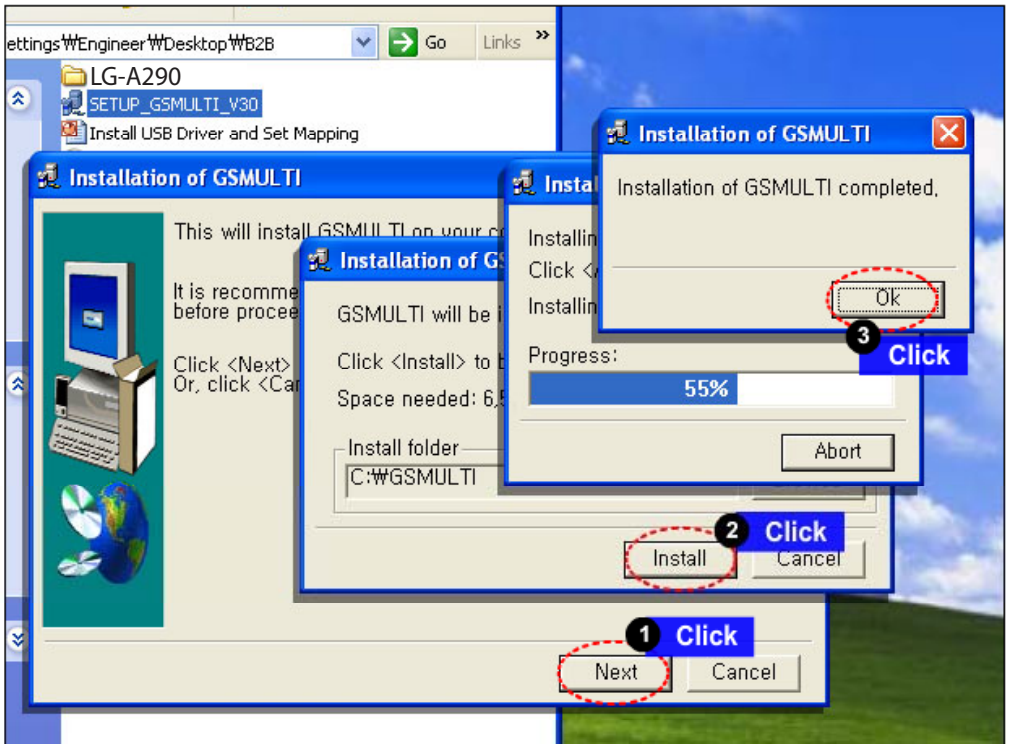
5. DOWNLOAD

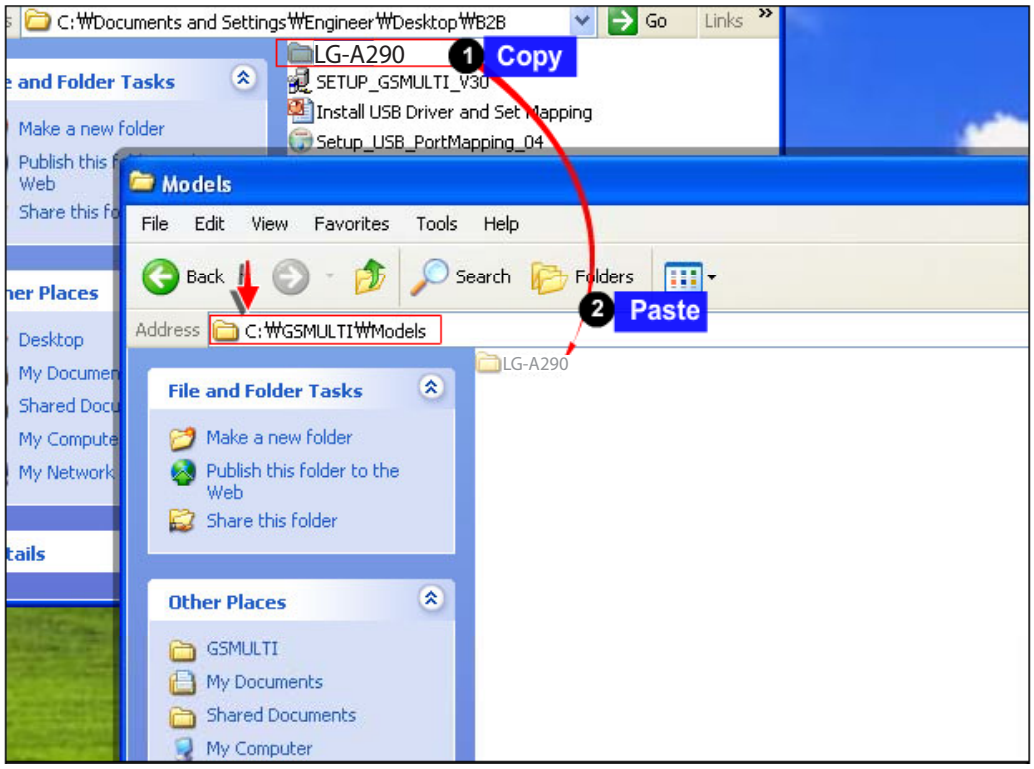


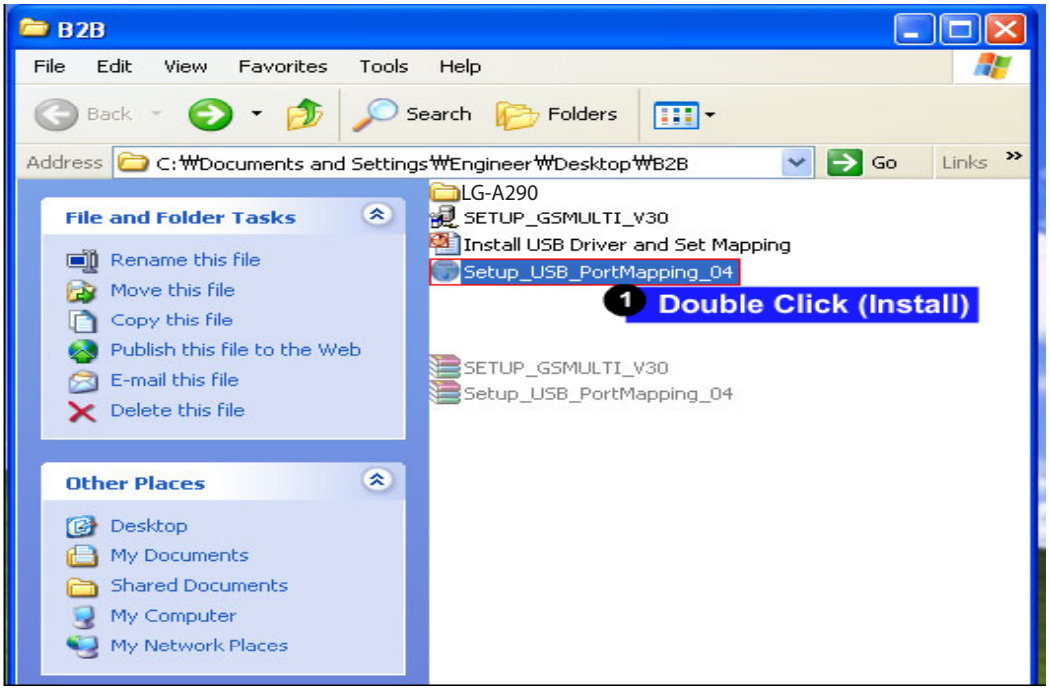


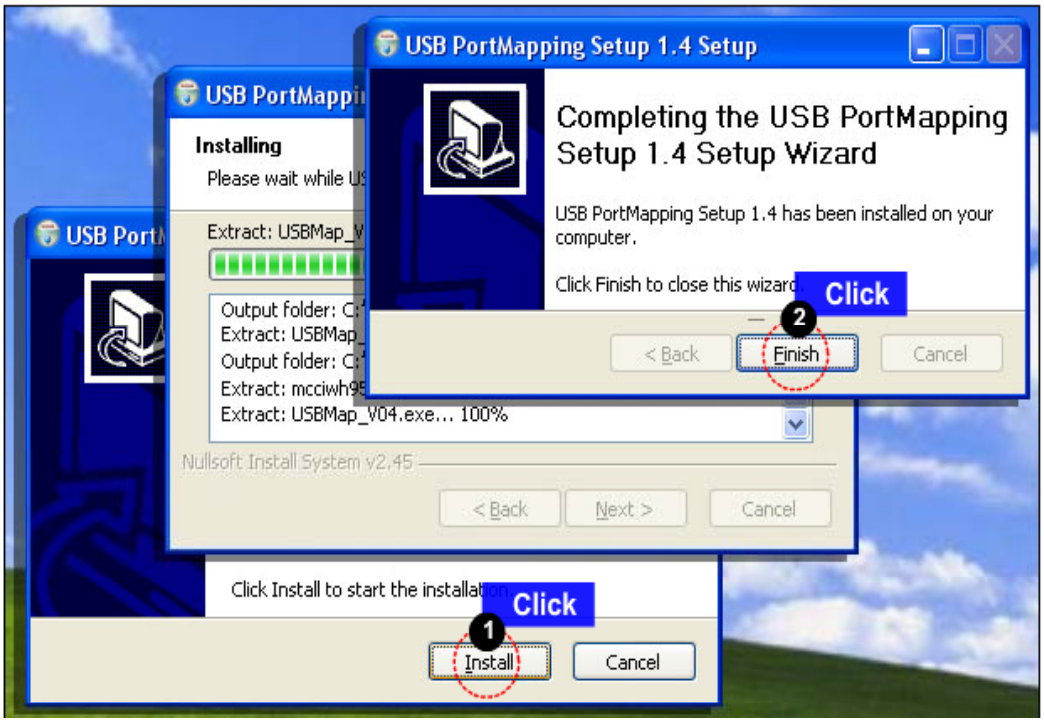


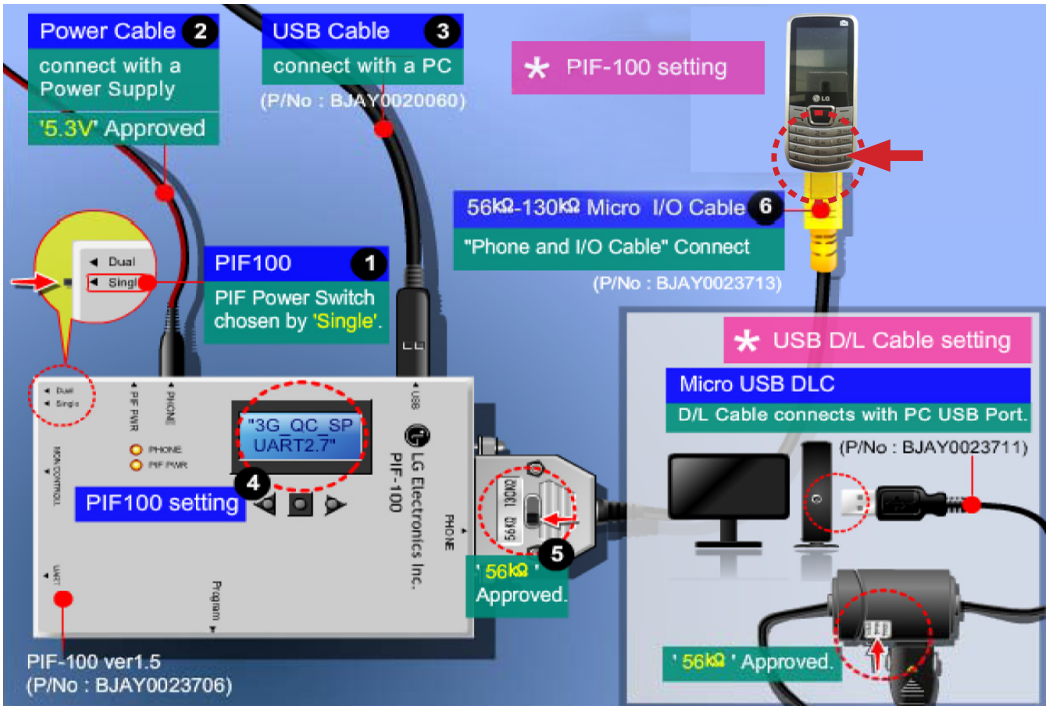


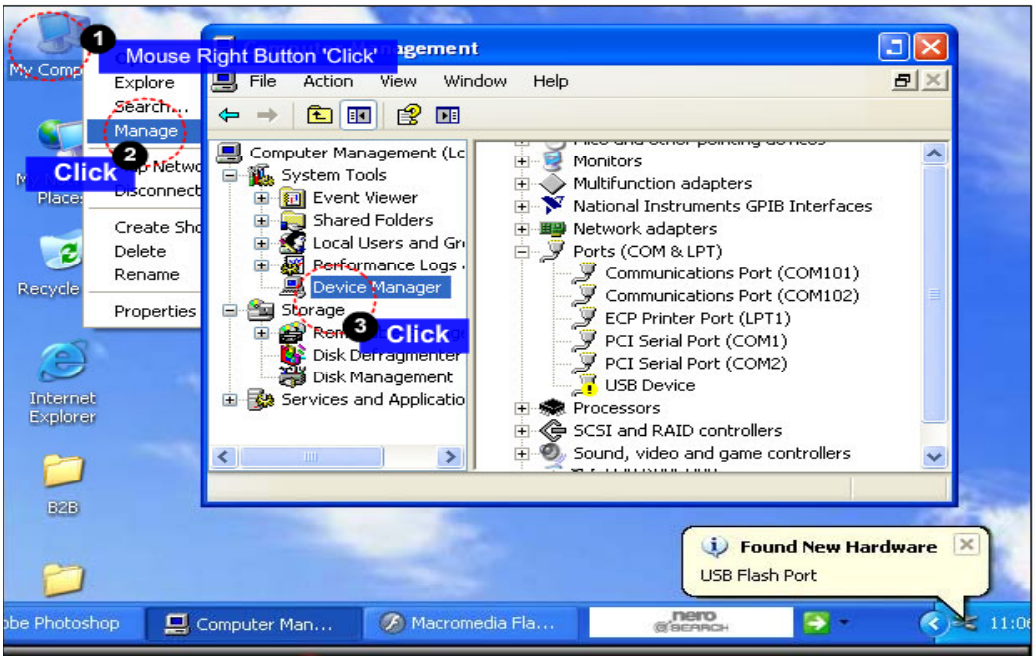


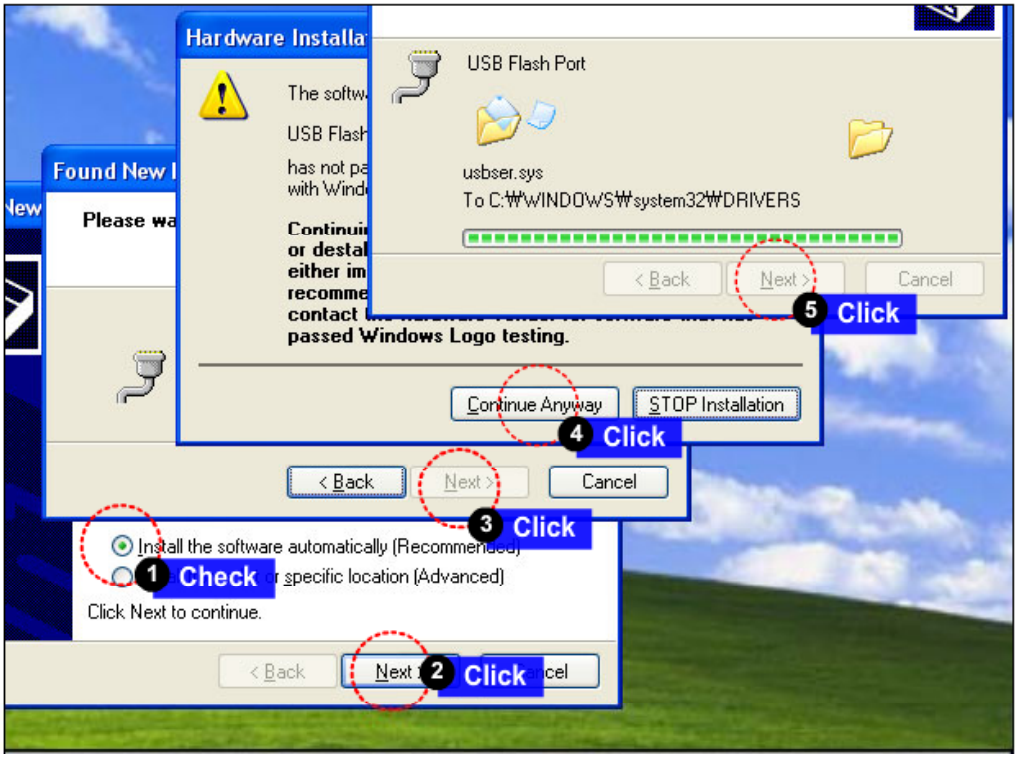


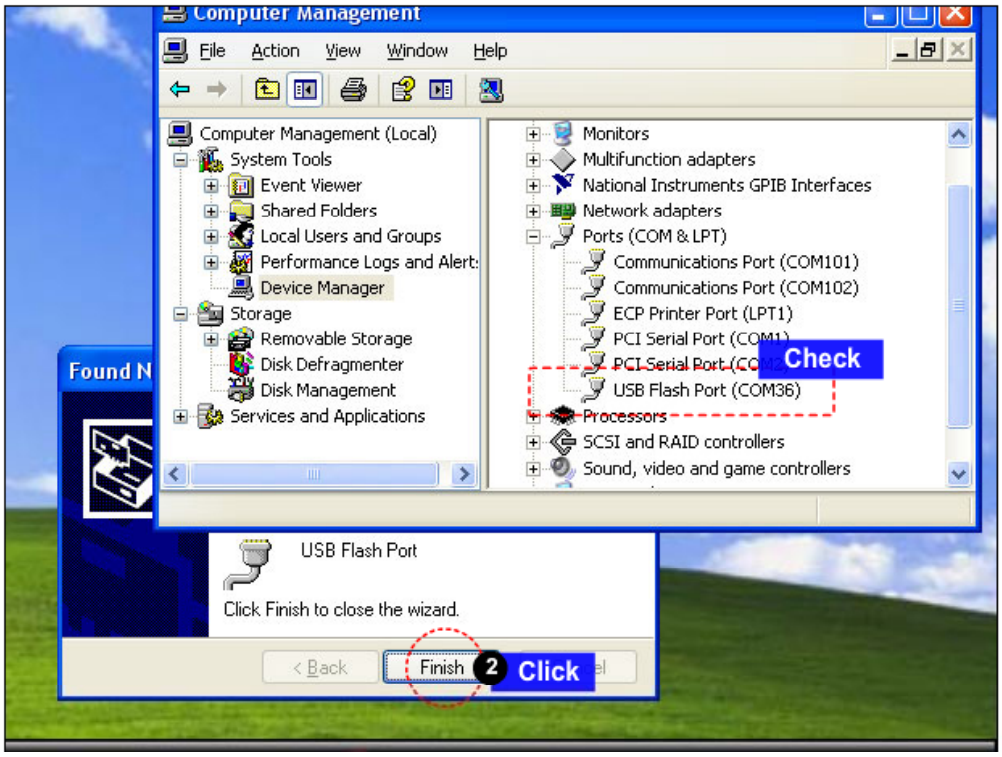


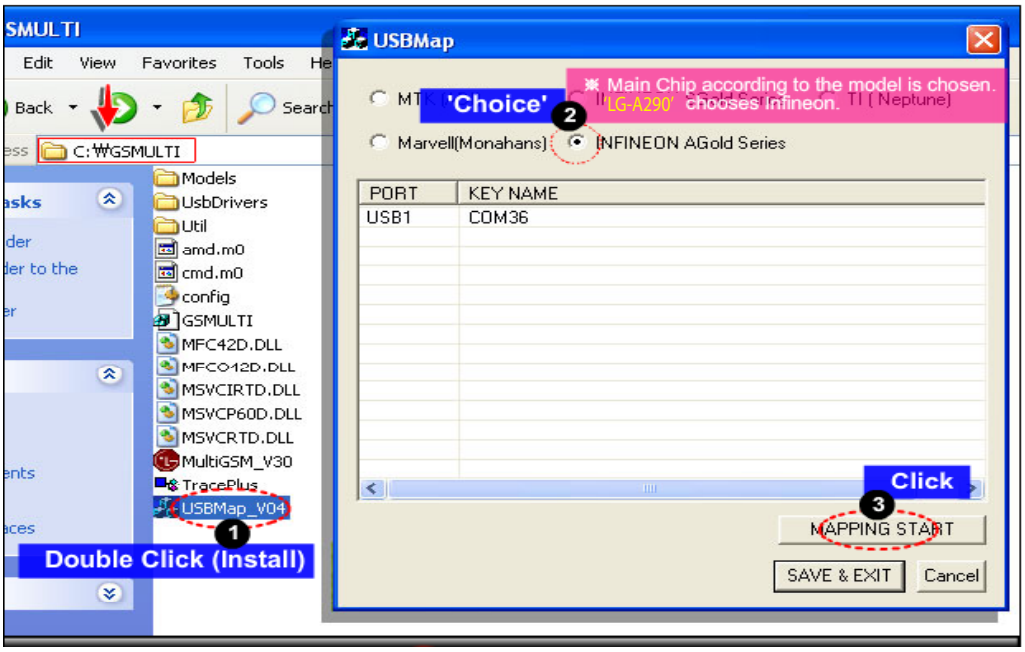


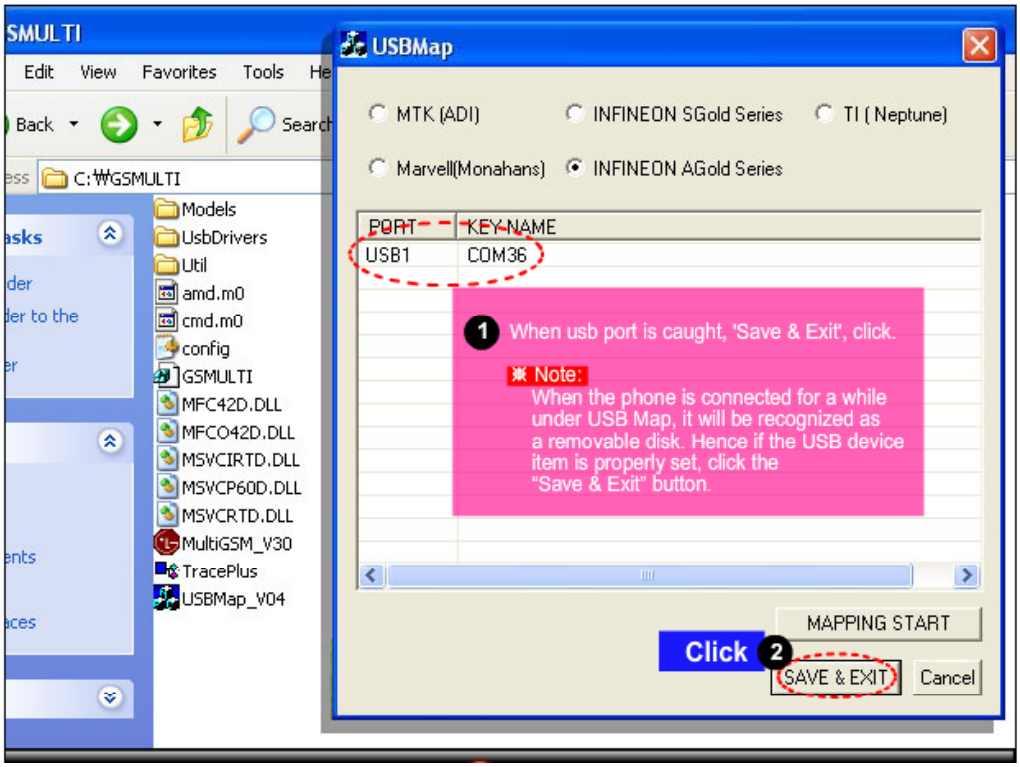


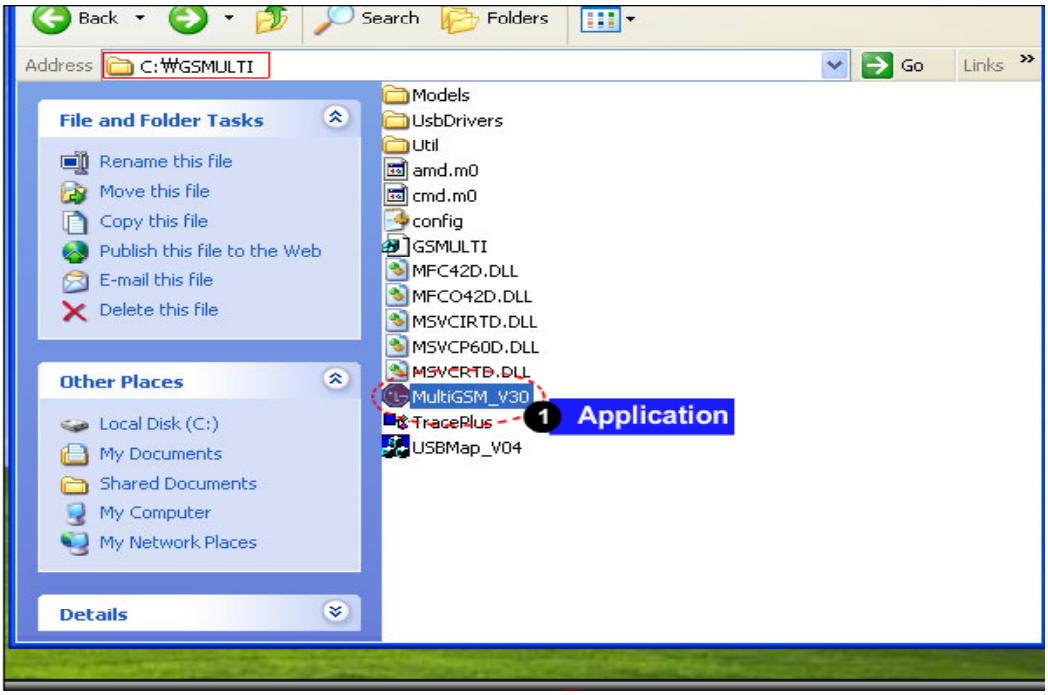


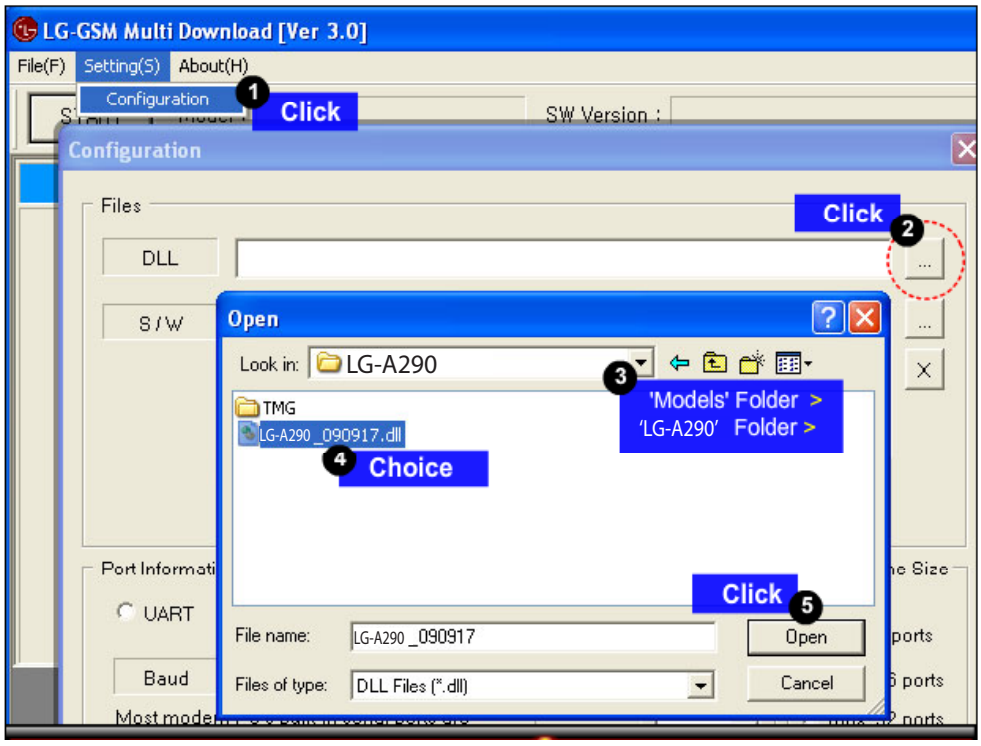


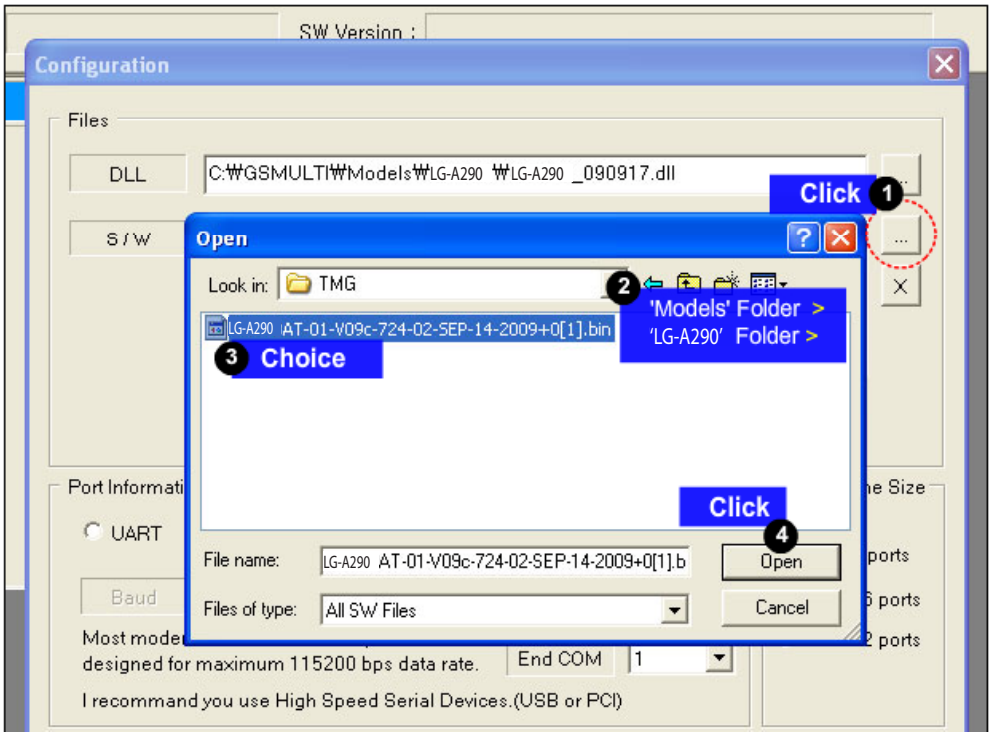


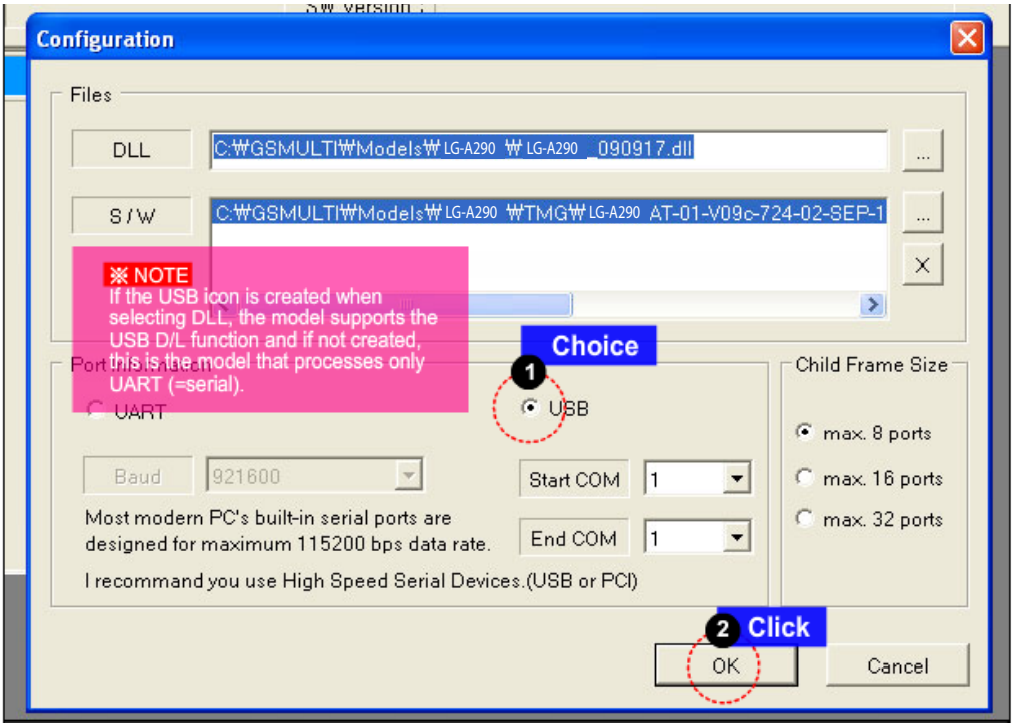


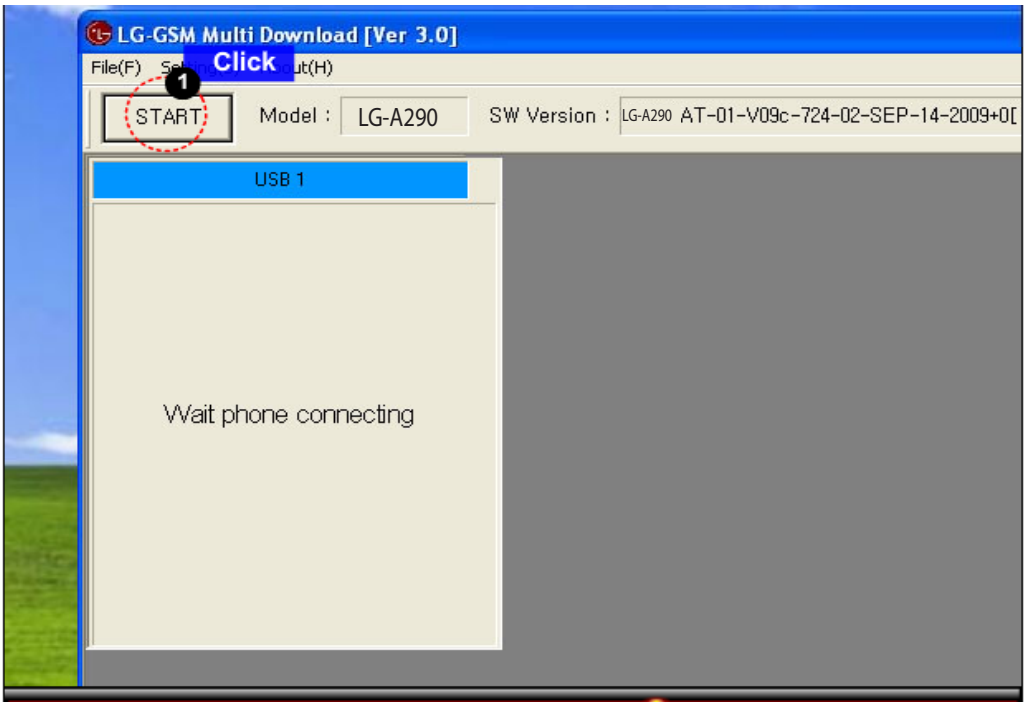


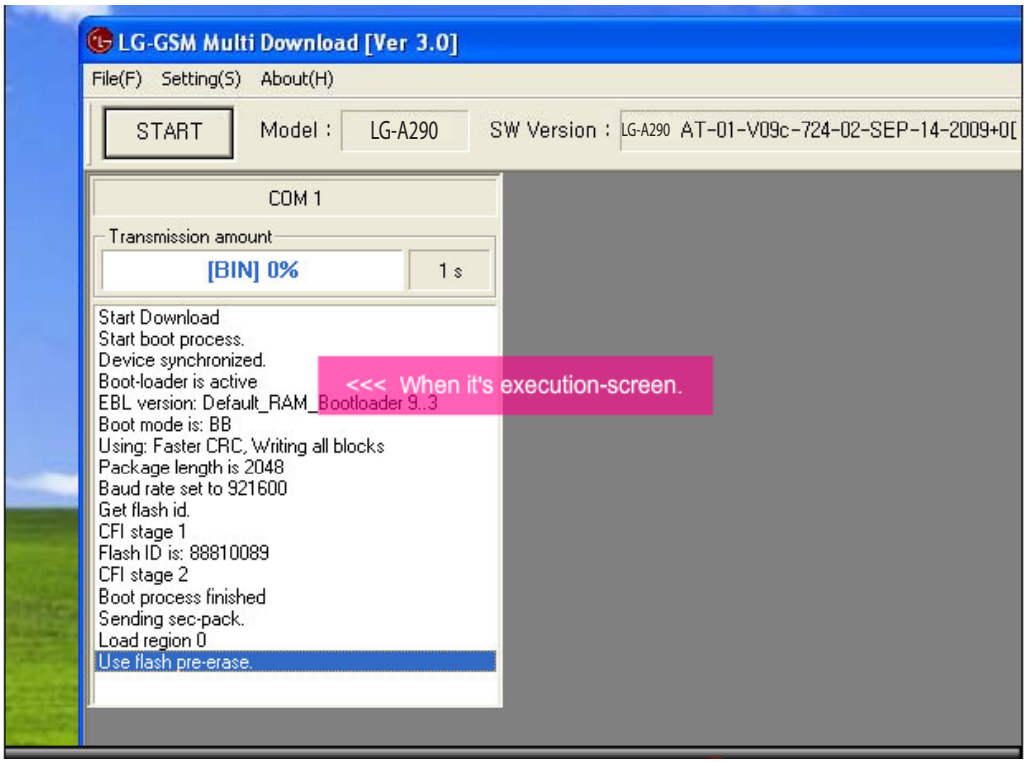


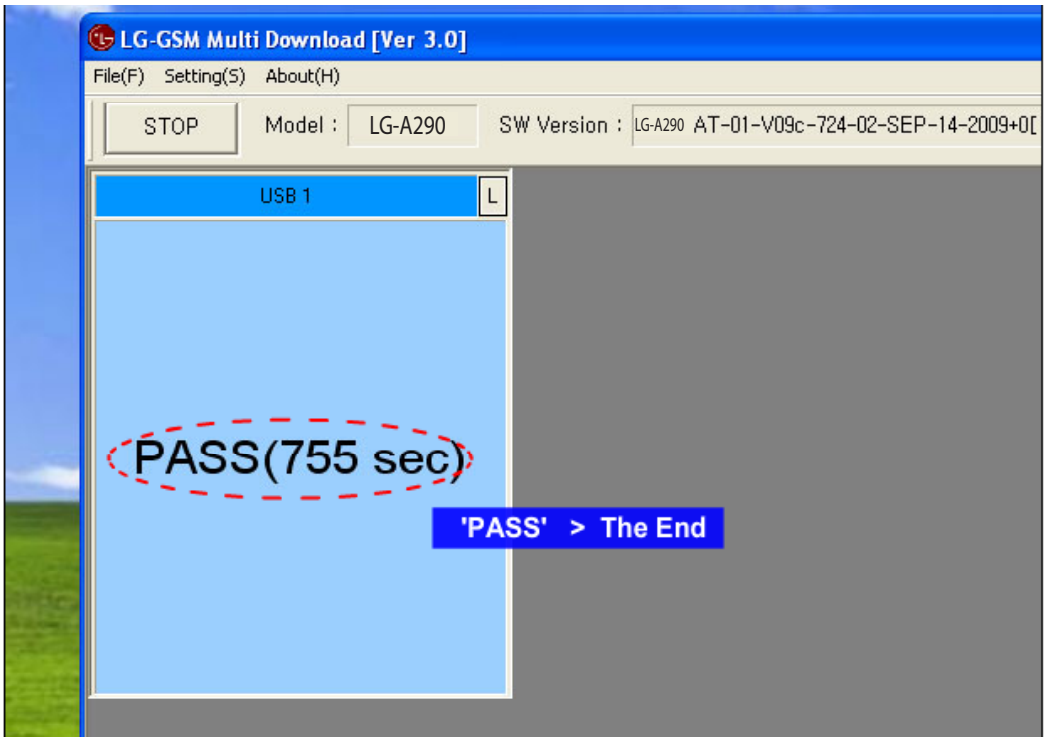






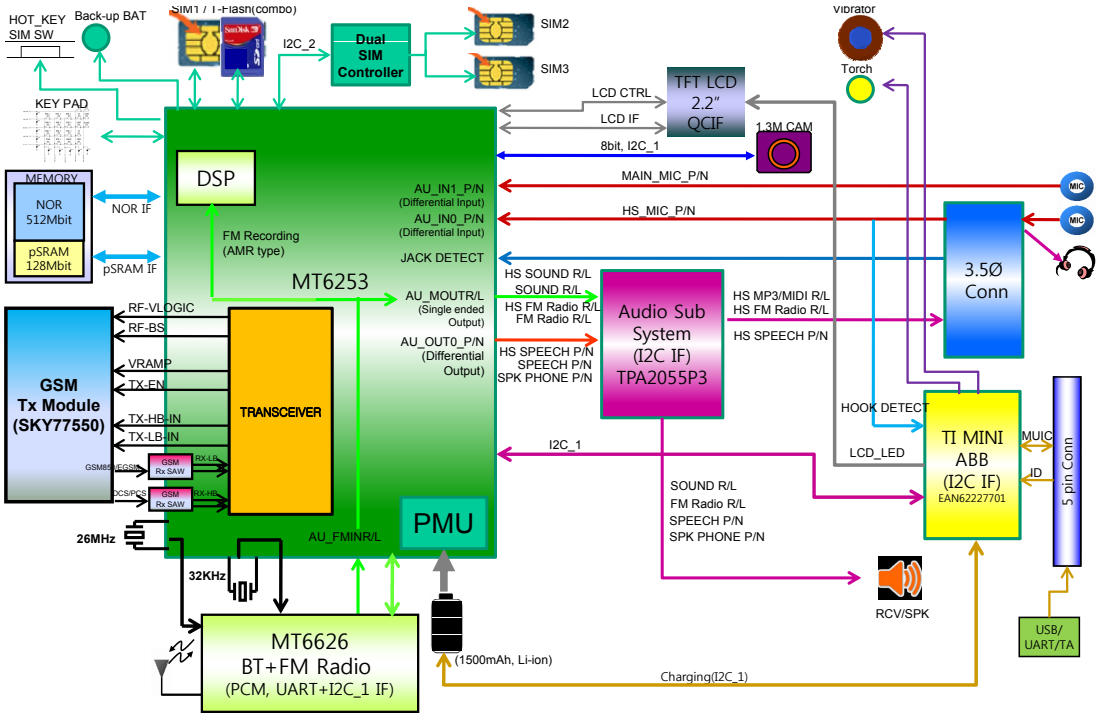




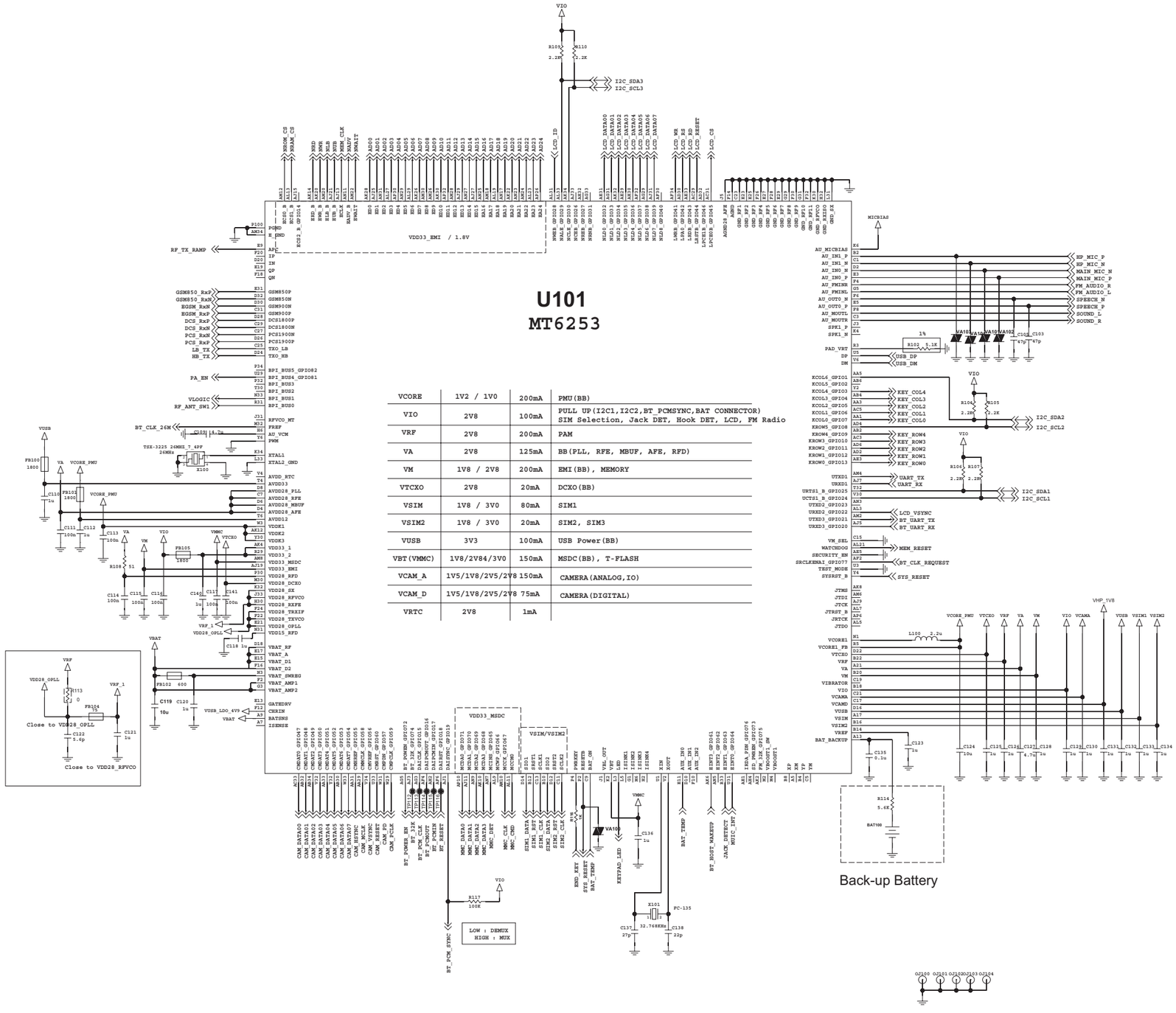


6. BLOCK DIAGRAM

AUDIO/SPEECH BLOCK DIAGRAM

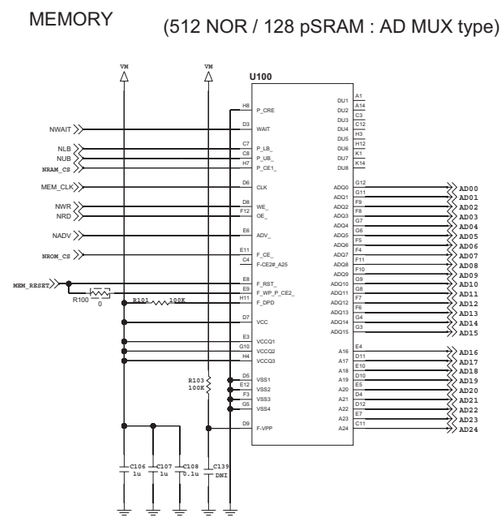


7. Circuit Diagram



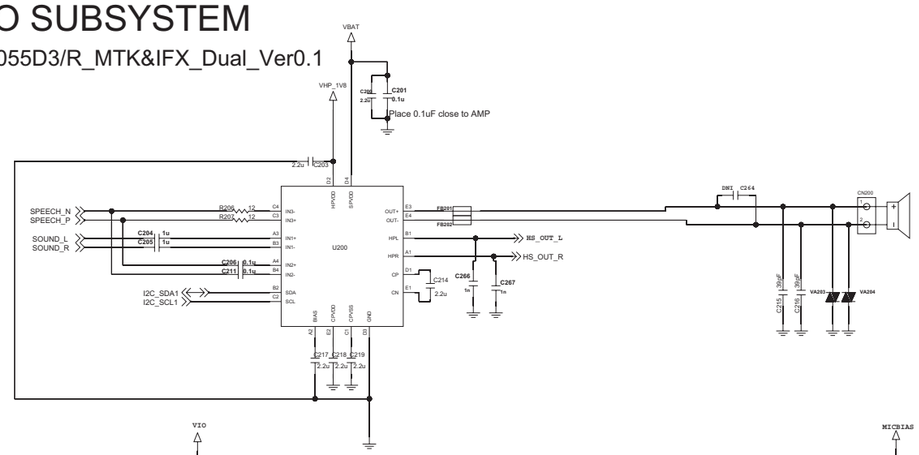
VCORE	1V2 / 1V0	200mA	PMU(BB)
VIO	2V8	100mA	PULL UP(I2C1,I2C2,BT_PCMSYNC,BAT CONNECTOR) SIM Selection, Jack DET, Hook DET, LCD, FM Radio
VRF	2V8	200mA	PAM
VA	2V8	125mA	BB(PLL, RFE, MBUF, AFE, RFD)
VM	1V8 / 2V8	200mA	EMI(BB), MEMORY
VTCXO	2V8	20mA	DCXO(BB)
VSIM	1V8 / 3V0	80mA	SIM1
VSIM2	1V8 / 3V0	20mA	SIM2, SIM3
VUSB	3V3	100mA	USB Power(BB)
VBT(VMMC)	1V8/2V84/3V0	150mA	MSDC(BB), T-FLASH
VCAM_A	1V5/1V8/2V5/2V8	150mA	CAMERA(ANALOG,IO)
VCAM_D	1V5/1V8/2V5/2V8	75mA	CAMERA(DIGITAL)
VRTC	2V8	1mA	

MEMORY (512 NOR / 128 pSRAM : AD MUX type)

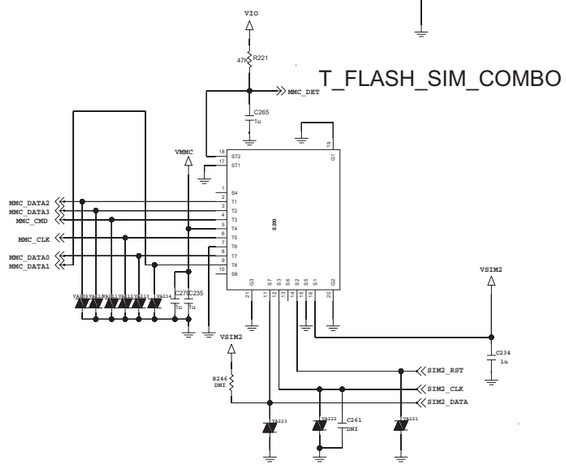


AUDIO SUBSYSTEM

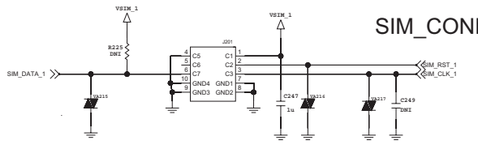
5-1-2-6_TPA2055D3/R_MTK&IFX_Dual_Ver0.1



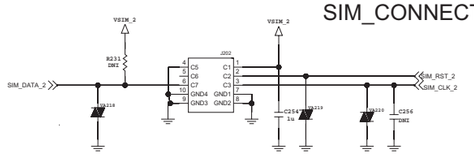
T_FLASH_SIM_COMBO



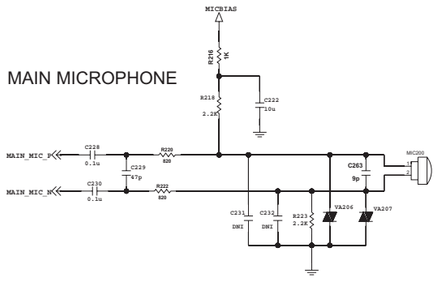
SIM_CONNECTOR



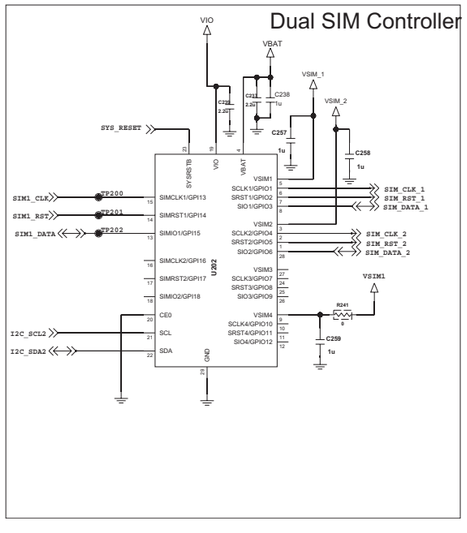
SIM_CONNECTOR



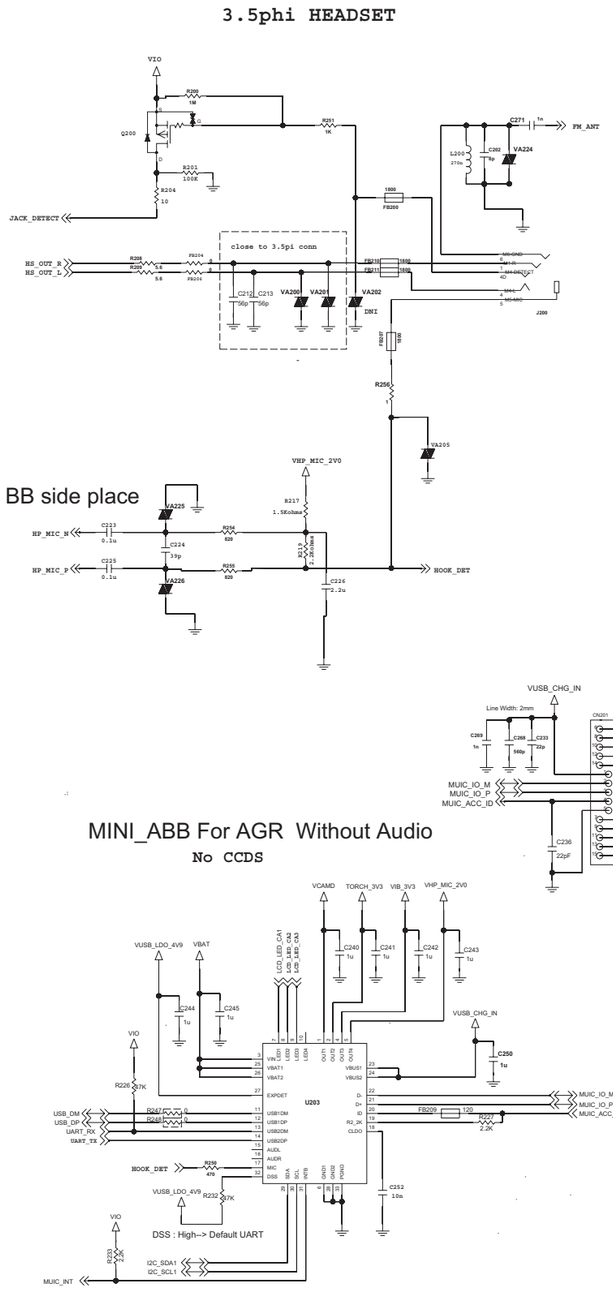
MAIN MICROPHONE



Dual SIM Controller



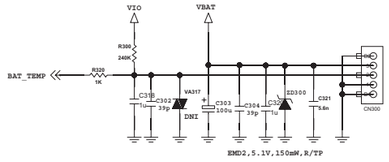
3.5phi HEADSET



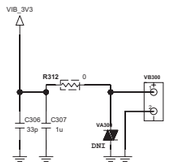
MINI_ABB For AGR Without Audio

No CCDS

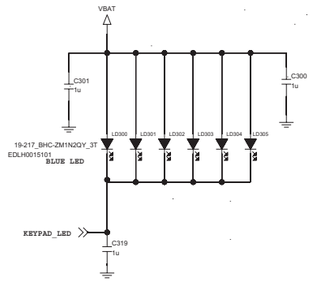
BATTERY CONNECTOR



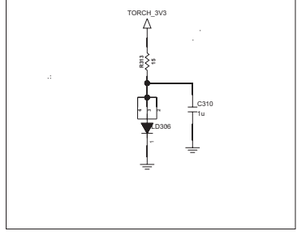
VIBRATOR



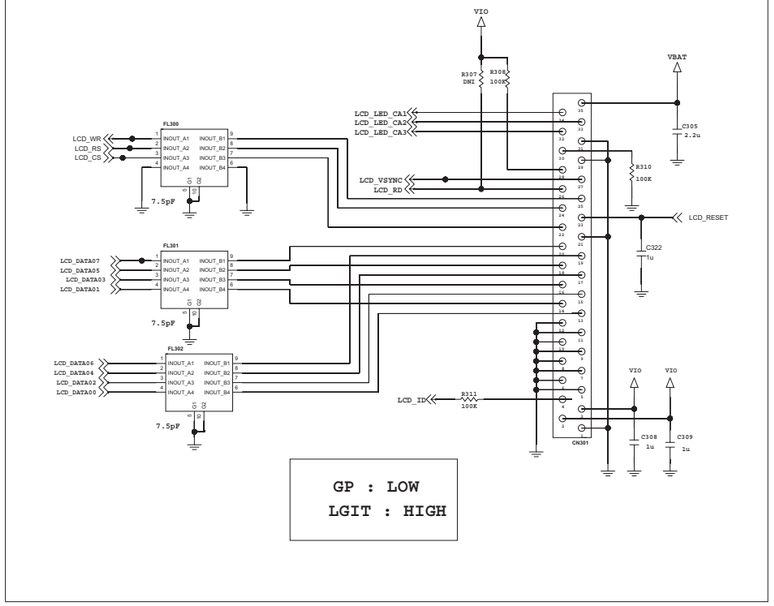
KEY BACKLIGHT



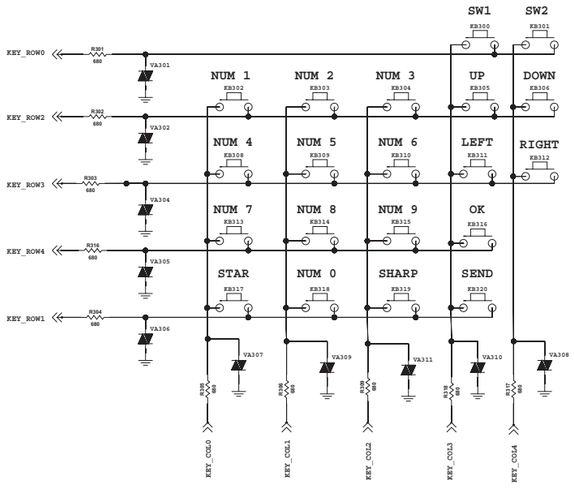
TORCH



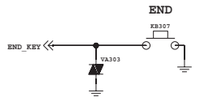
LCD INTERFACE CONNECTOR

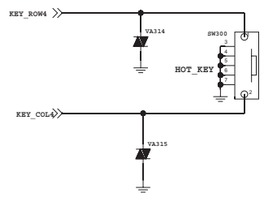


KEYPAD INTERFACE

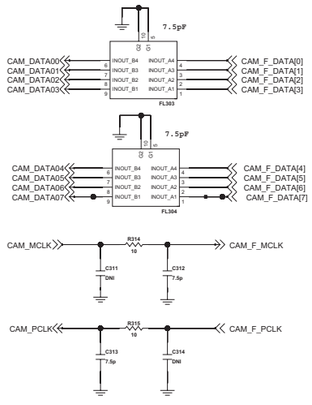


END

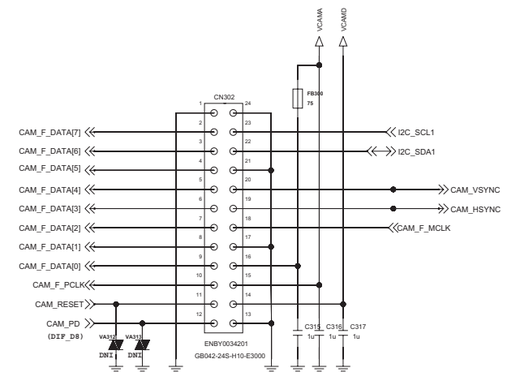




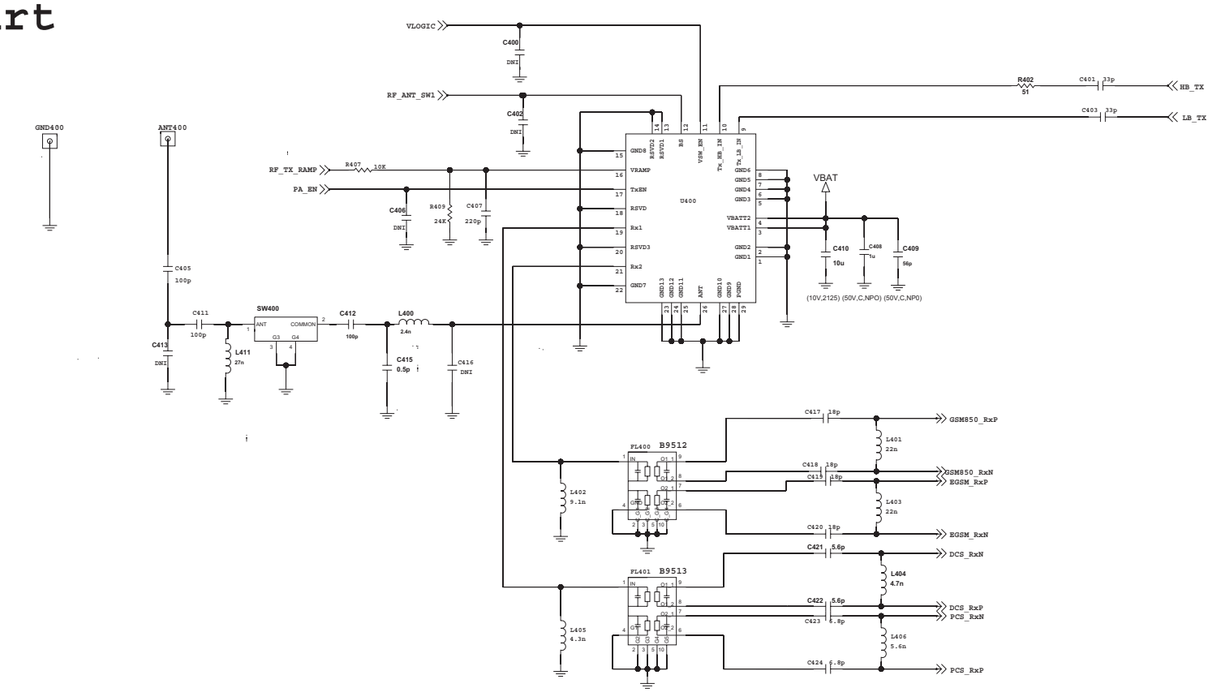
EMI FILTER



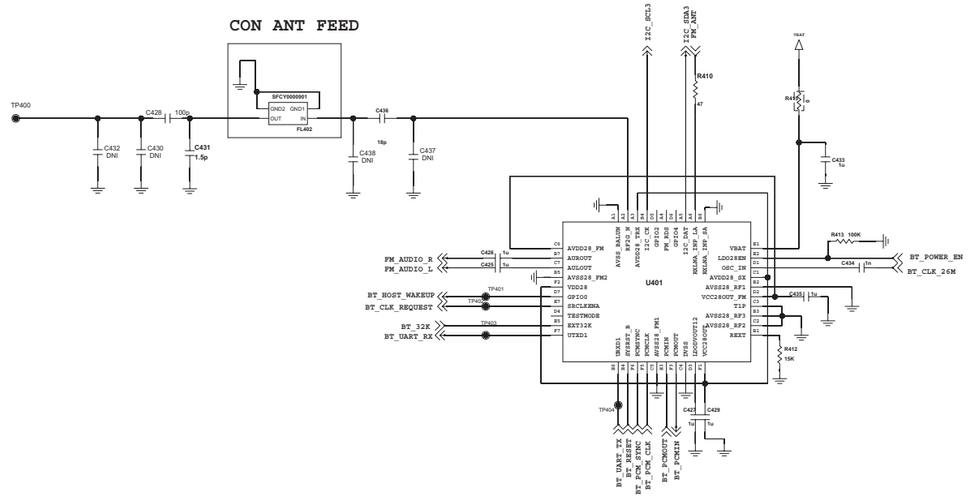
CAM CONN



RF Part

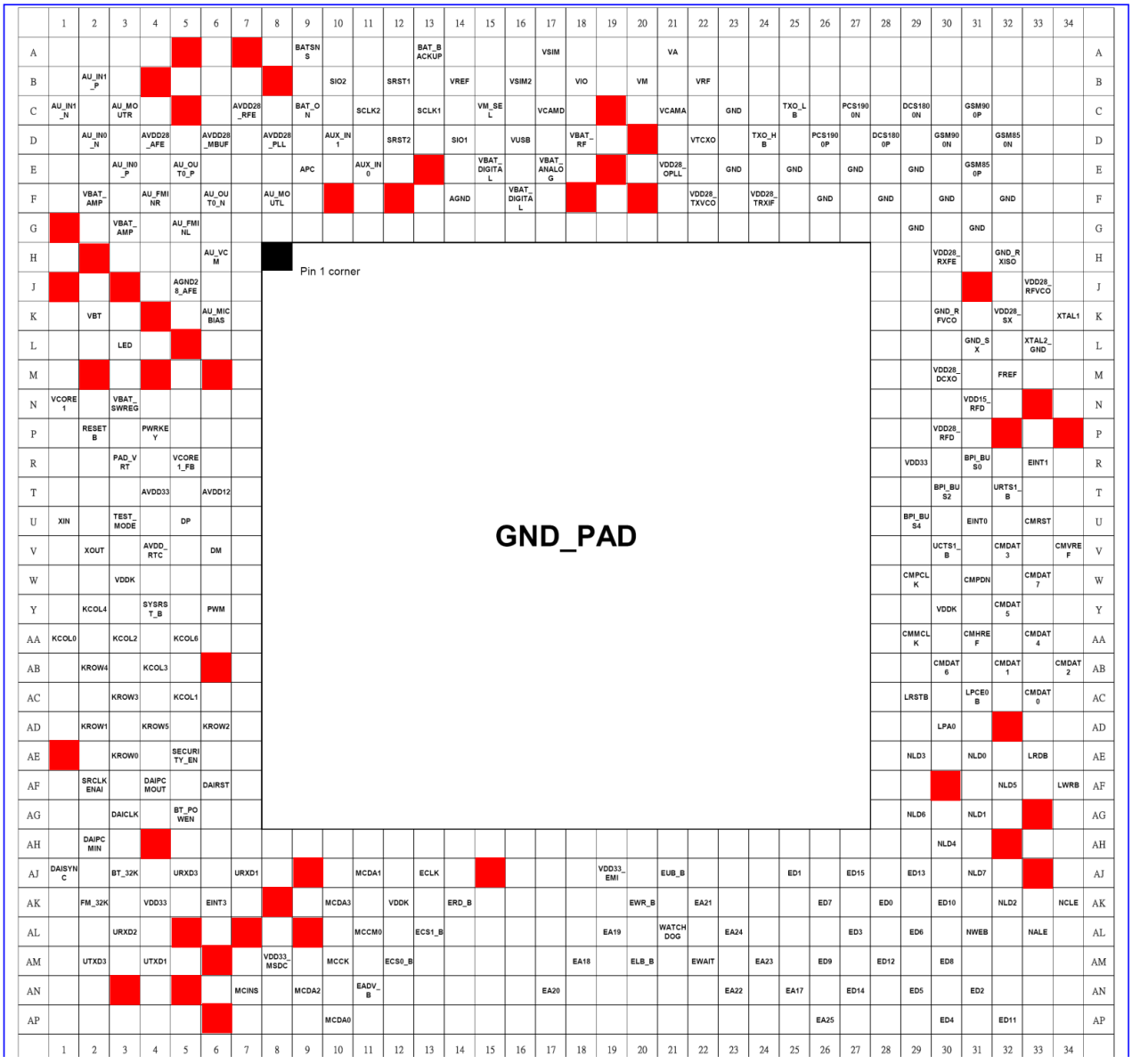


BT & FM



8.BGA PIN MAP

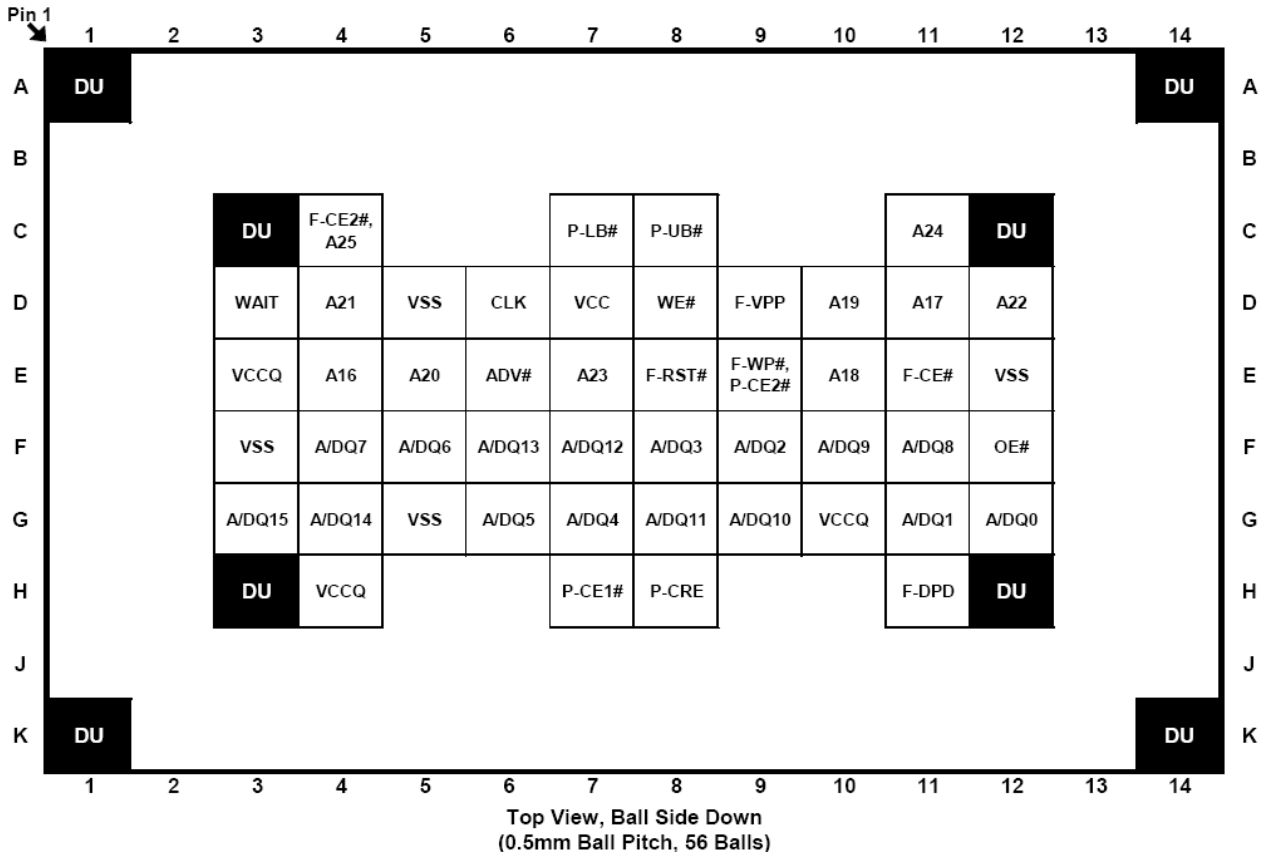
BGA IC pin check (U101)



: not in use

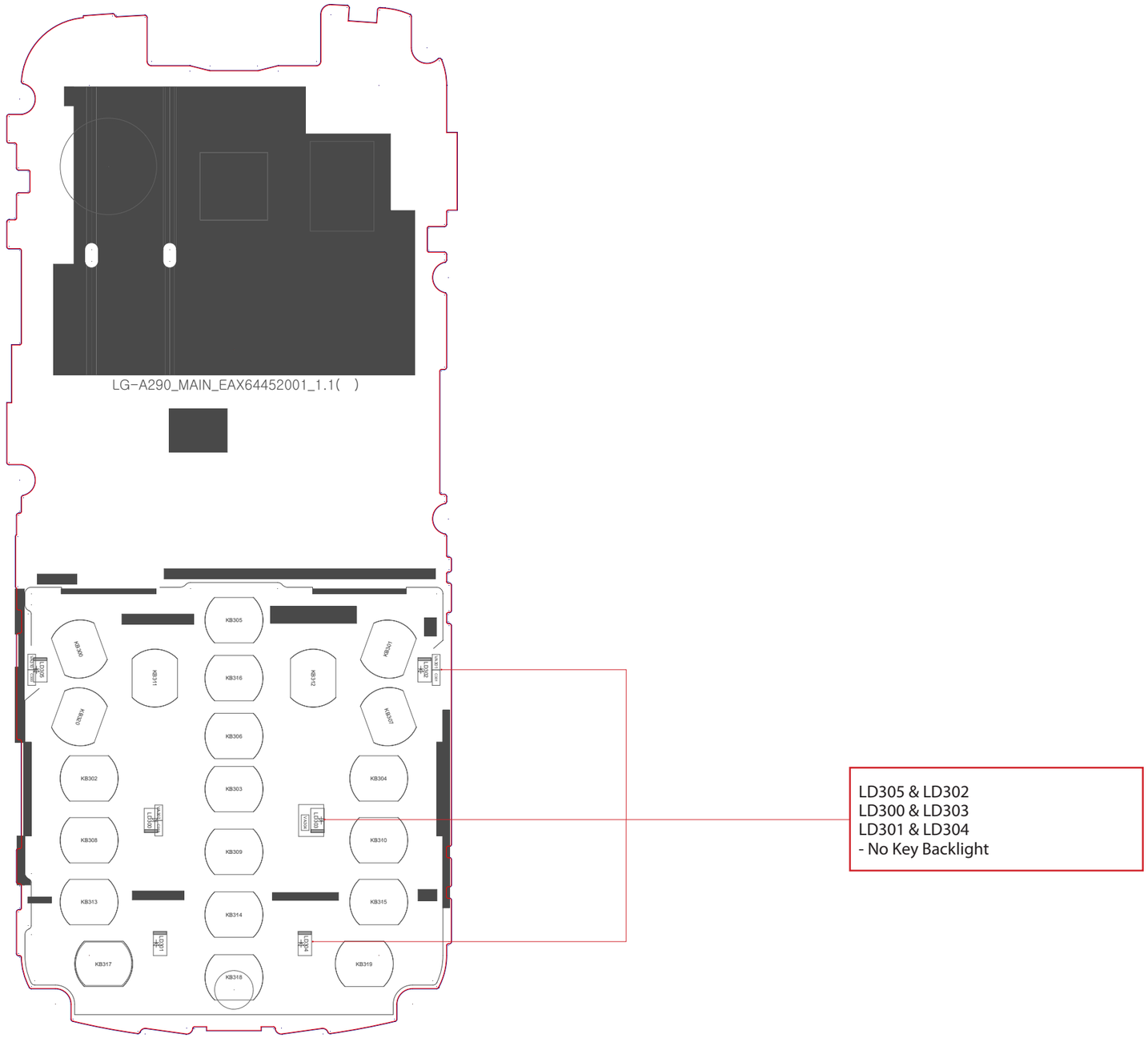
BGA IC pin check (U100)

■ Ball Diagram (Top View), PF38F5060M0Y3DK



■ **: not in use**

9. PCB LAYOUT



LG-A290_MAIN_EAX64452001_1.1_TOP

J200(3.5φ Headset)
- No 3.5φ Headset

CN302(Camera connector)
- No Camera

U203(miniABB)
- No Charging
- No USB
- No LCD Backlight

CN301(LCD connector)
- No LCD Display

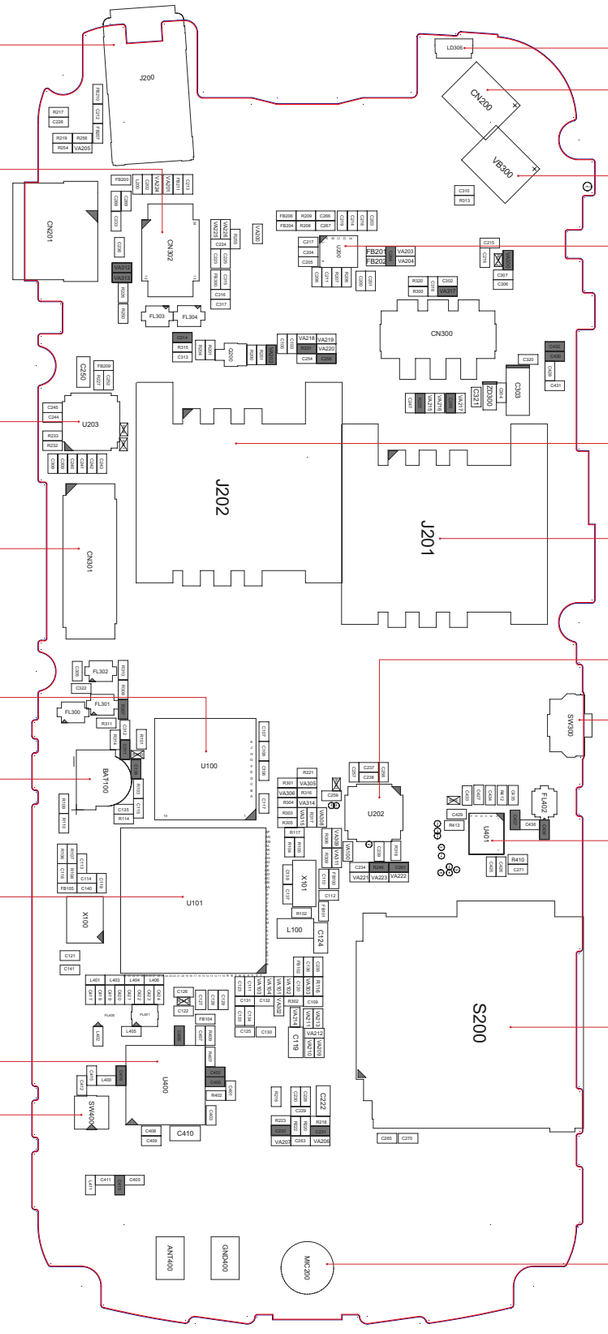
U100(Memory)
- No booting

BAT100(Backup Battery)
- No service

U101(DBB)
- No Power on
- No service

U400(RF module)
- RF sensitivity
- Tx Power
- No service

SW400(mobile switch)
- Can't make a call
- Tx Low power
- Not good BER
- No Service



LD306(Torch LED)
- No Torch

CN200(Speaker PAD)
- No Speaker

VB300(Vibrator PAD)
- No Vibrator

U200(Audio sub system)
- The Audio working bad

J202(SIM3 socket)
- No SIM3 operation

J201(SIM2 socket)
- No SIM2 operation

U202(Dual SIM controller)
- No SIM2, SIM3 operation

SW300(SIM switch)
- No SIM change operation

U401(BT/FM)
- The FM Radio working bad (in use intenna)
- The Bluetooth working bad

S200(T-flash/SIM1 combo)
- No SIM1 operation
- No u-SD Memory

MIC200
- No MIC operation

LG-A290_MAIN_EAX64452001_1.1_BOT

10. ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "3845#*290# "Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

[1] Device Test
- **[1-1] All Auto Test**
- **[1-2] All Auto Test Result**
- **[1-3] Auto Detect**
- **[1-4] Key Press Test**
- **[1-5] Camera Test**
- **[1-6] Display Test**
- **[1-7] Sound Test**
- **[1-8] Vibrator Test**
- **[1-9] Acoustic loopback**
- **[1-10] FM Radio**
- **[1-11] Torch Test**
- **[1-12] LCD Backlight**
- **[1-13] Keypad Backlight**
- **[1-14] Vibrator Duration**
- **[1-15] LCD**

[2] ELT mode
- **[2-1] Automatic**
  - [2-1-1] 1 Time
  - [2-1-2] 2 Times
  - [2-1-3] 3 Times
  - [2-1-4] 4 Times
  - [2-1-5] 5 Times
  - [2-1-6] 25 Times
  - [2-1-7] 100 Times
  - [2-1-8] Infinite Times
- **[2-2] Manual**
  - [2-2-1] LCD backlight
  - [2-2-2] Ringtone
  - [2-2-3] Vibrator
  - [2-2-4] Camera
  - [2-2-5] Audio loopback

[3] SW sanity test
- **[3-1] FPRI Test**
- **[3-2] E serial NO**
- **[3-3] UA string**
- **[3-4] UA profile**
- **[3-5] Unlock SIM**
- **[3-6] DB Check**
  - [3-6-1] Copy to user disk
  - [3-6-2] Copy to Ext disk
  - [3-6-3] CRC

[4] Factory Reset

[5] Call Timer

[6] Version

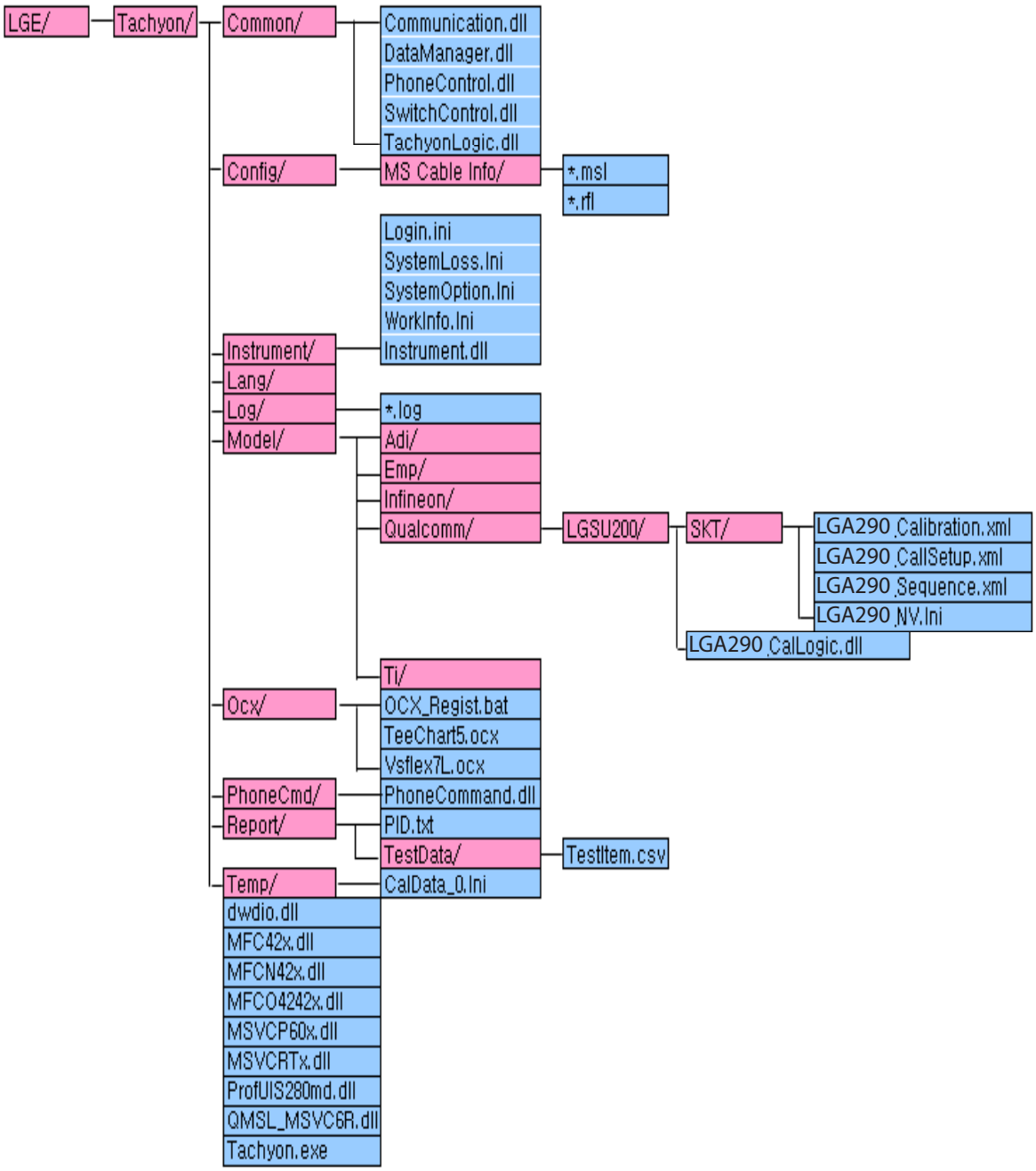
[7] Resource BIN
- **[1-1] LANGPACK**
- **[1-2] CUSTPACK**

[8] Engineer Mode
- **[8-1] Network Setting**
  - [8-1-1] Network Info
  - [8-1-2] Band Selection
  - [8-1-3] PLMN list preference
- **[8-2] Device**
  - [8-2-1] LCD
  - [8-2-2] GPIO
  - [8-2-3] PWM
  - [8-2-4] EINT
  - [8-2-5] ADC
  - [8-2-6] Set Default Level
  - [8-2-7] Set UART
  - [8-2-8] Sleep Mode
  - [8-2-9] DCM Mode
  - [8-2-10] Memory Info
  - [8-2-11] FM Radio
  - [8-2-12] PMU register settings
- **[8-3] GPRS Act**
  - [8-3-1] Attach
  - [8-3-2] 1st PDP
  - [8-3-3] 2nd PDP
- **[8-4] Packet Data Connect**
  - [8-4-1] SIM Slot1 Empty
  - [8-4-2] SIM Slot2 Empty
  - [8-4-3] SIM Slot3 Empty
- **[8-5] Debug Info**
  - [8-5-1] last Exception
- **[8-6] Bluetooth**
  - [8-6-1] General Test
  - [8-6-2] Bluetooth RF Test
  - [8-6-3] Bluetooth UPF Test
  - [8-6-4] A2 BT Test
- **[8-7] Enable Fake Lang**
- **[8-8] Heap freesize**

11RF CALIBRATION

11.1 Configuration of Tachyon

11.1.1 Configuration of directory



11.1.2 Description of basic folders

Folder	Description
Tachyon	Exe file and MFC dll, UI dll is present.
Common	Common dll files. (XML Data I/O , Auto Test Logic, Tachyon Logic Control, Communication)
Config	Envirement files. (Port configuration, Loss adjust)
Instrument	Tester control dll.
Model	Model files is present. (Model -> Solution (Qualcomm, EMP, ADI, INFINEON) -> MODEL NAME(LGGM630, LGSH470, ..) -> BUYER NAME(SKT, TEL, VIVO, …)
OCX	Conponent files.
PhoneCmd	Phone communication file
Report	Report Files is present. (Cal data, test data)

11.1.3 Description of configuration files

File	Description
'MODEL NAME'_Calibration.XML	There are imformations to calibrate. It consist of calibration items.
'MODEL NAME'_CallSetup.XML	There are imformations to call.
'MODEL NAME'_NV.INI	It consists of default values. It is written when 'cal&auto' is begun.
'MODEL NAME'_Sequence.XML	It is described a testing procedures.

11.2 How to use Tachyon

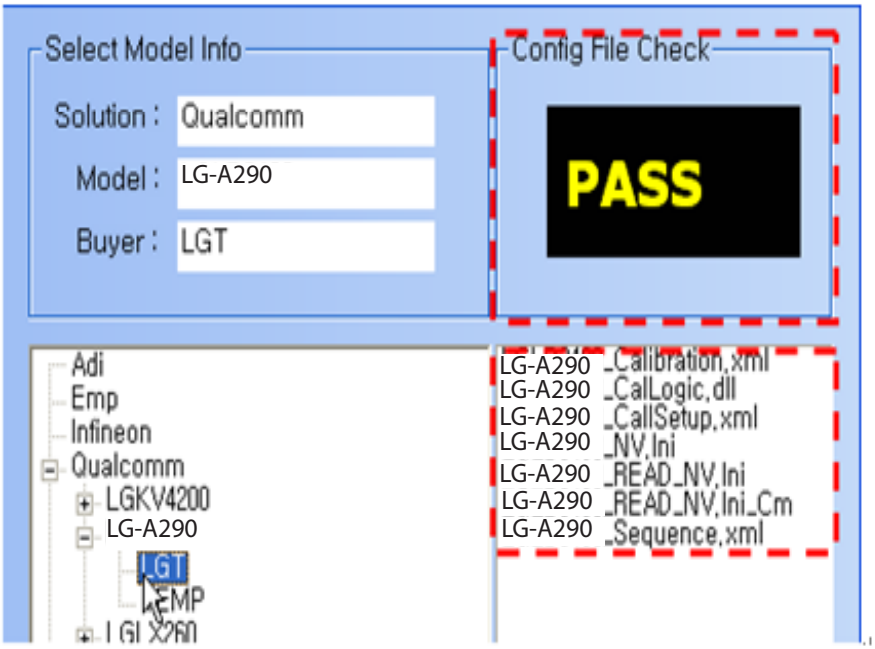
11.2.1 Model selection

Follow the procedure before start calibration & auto test

a. Click the icon,  in tool bar.

Then, You can make a choice of LG-A290 for loading cfg files before run.

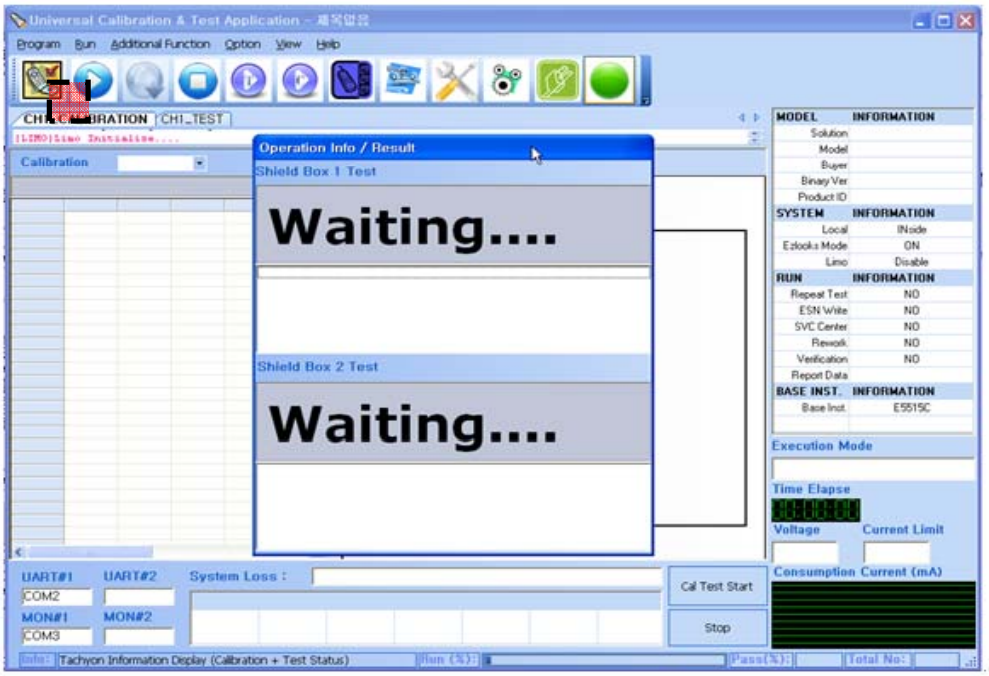
b. Select model name and then do double-click the buyer name.
You will see configuration files loaded in the right window with PASS information above



< Example of selection of model name>

11.2.2 Start cal & auto

a. Click calibration & autotest button,  in Tool bar

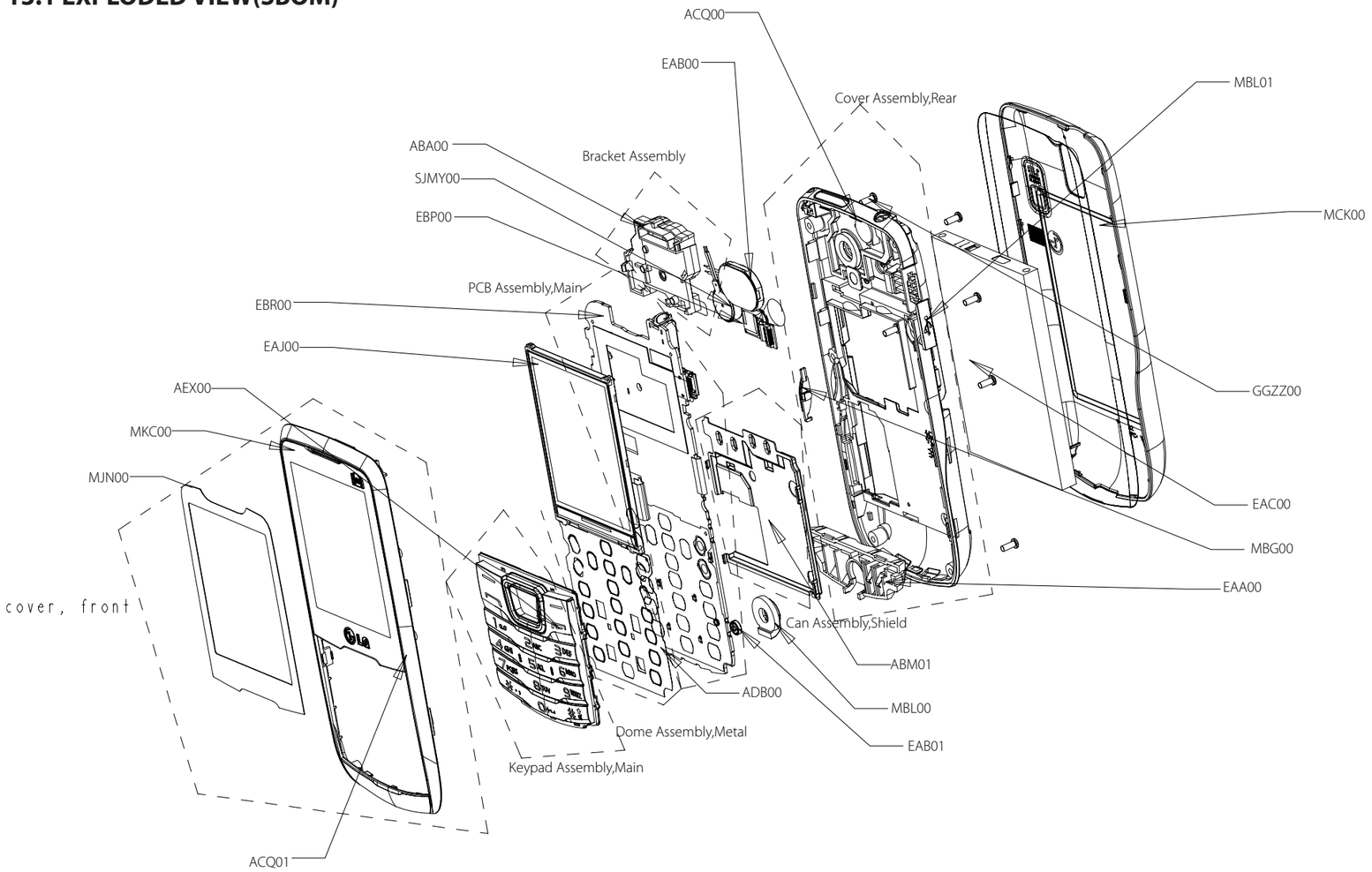


b. Calibration & autotest will be executed in order.

1) Precede Action.
- NV write
- Test command send.
2) RF Calibration
3) RF Auto test
4) After action
- Phone reset
- Change UE to AMSS

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.1 EXPLODED VIEW(SBOM)



Location	Description
EBR00	PCB Assembly,Main
SJMY00	Motor,DC
ABA00	Bracket Assembly
ABM01	Can Assembly,Shield
ADB00	Dome Assembly,Metal
EAB00	Speaker,Dual Mode
EAJ00	LCD Module
EBP00	Camera Module
EAB01	Microphone,Condenser
GGZZ00	Screw,Tapping
ACQ00	Cover Assembly,Rear
MBG00	Button,Side
MBL00	Cap
MBL01	Cap,Receptacle
EAA00	PIFA Antenna,Multiple
ACQ01	Cover Assembly,Front
MJN00	Tape,Window
MKC00	Window,LCD
AEX00	Keypad Assembly,Main
MCK00	Cover,Battery
EAC00	Rechargeable Battery,Lithium Ion

12.2 ReplacementParts <Mechanic component>

Note: This Chapterisused for reference,Part order is ordered by SBOM standard on GCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
1	AGQ000000	Phone Assembly	AGQ86713301	LGA290.ABRASV SV:SILVER SILVER -	
2	ACQ100400	Cover Assembly,EMS	ACQ85944501	LGA290.ABRASV SV:SILVER SILVER -	
5	ABA00	Bracket Assembly	ABA74130801	LGA290.ABRAZY BK:Black -	
6	MAZ000000	Bracket	MAZ63334801	MOLD PC LGA290.ABRAZY BK:Black -	
6	MJN000000	Tape	MJN68004101	COMPLEX LGA290.ABRAZY BK:Black -	
6	MJN009400	Tape,Camera	MJN68003901	COMPLEX LGA290.ABRAZY BK:BLACK BLACK -	
6	MCQ074200	Damper,Speaker	MCQ66906201	COMPLEX LGA290.ABRAZY BK:Black -	
5	MJN000002	Tape	MJN68132901	COMPLEX LGA290.ABRAZY ZZ:Without Color -	
5	MJN000001	Tape	MJN68093701	COMPLEX LGA290.ABRAZY ZZ:Without Color -	
5	ABM01	Can Assembly,Shield	ABM73677101	LGA290.ABRAZY BK:Black -	
5	ADB00	Dome Assembly,Metal	ADB73778401	LGA290.ABRAZY BK:Black -	
5	MEV000000	Insulator	MEV63977601	COMPLEX LGA290.ABRAZY BK:Black -	
5	MJN000000	Tape	MJN67977501	COMPLEX LGA290.ABRAZY BK:Black -	
5	MEZ000000	Label	MLAZ0038301	COMPLEX LG-VX6000 ZZ:Without Color PID Label 4 Array PRINTING,	
3	GGZZ00	Screw,Tapping	GGZZ0004901	GGZZ0004901 BH + - 1.6mM 4mM SWCH FZB SERVEONE CO., LTD.	
3	ACQ00	Cover Assembly,Rear	ACQ85749801	LGA290.ABRAZY BK:Black -	
4	MBG00	Button,Side	MBG64406301	MOLD PC LUPOY SC-1004A LGA290.ABRAZY BK:Black -	

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	MBL00	Cap	MBL65136901	COMPLEX LGA290.ABRAZY BK:Black -	
4	MBL01	Cap,Receptacle	MBL65137001	MOLD RUBBER LGA290.ABRAZY BK:Black -	
4	MCK063300	Cover,Rear	MCK66962301	MOLD PC LUPOY SC-1004A LGA290.ABRAZY BK:Black -	
4	MCQ009400	Damper,Camera	MCQ66816701	COMPLEX LGA290.ABRAZY BK:Black -	
4	MCQ015700	Damper Connector	MCQ66816801	COMPLEX LGA290.ABRAZY BK:Black -	
4	MEZ002100	Label,After Service	MLAB0001102	COMPLEX C2000 CGRSV WA:White C2000 USASV DIA 4.0 PRINTING,	
4	MJN061100	Damper,Motor	MCQ66837601	COMPLEX LGA290.ABRAZY BK:Black -	
4	MKC009400	Window,Camera	MKC64201401	CUTTING PMMA LGA290.ABRAZY BK:Black -	
4	MKC041800	Window,IRDA	MKC64180701	CUTTING PC LGA290.ABRAZY TR:Transparent -	
4	MJN089300	Tape,Window	MJN68004001	COMPLEX LGA290.ABRAZY BK:Black -	
4	MDJ000000	Filter	MDJ63324201	COMPLEX LGA290.ABRAZY BK:Black -	
4	MCQ000000	Damper	MCQ66837701	COMPLEX LGA290.ABRAZY BK:Black -	
3	ACQ01	Cover Assembly,Front	ACQ85744801	LGA290.ABRAZY BK:Black -	
4	MJN00	Tape,Window	MJN68003801	COMPLEX LGA290.ABRAZY BK:Black -	
4	MDJ000000	Filter	MDJ63286501	COMPLEX LGA290.ABRAZY BK:Black -	
4	MCQ043300	Damper,LCD	MCQ66816501	COMPLEX LGA290.ABRAZY BK:Black -	
4	MCK032700	Cover,Front	MCK66981901	MOLD PC LUPOY SC-1004A LGA290.ABRAZY BK:Black -	
4	MCR000000	Decor	MCR64734501	COMPLEX LGA290.ABRASV ZZ:Without Color -	
4	MKC00	Window,LCD	MKC64180501	CUTTING PMMA LGA290.ABRAZY BK:Black -	
3	AEX00	Keypad Assembly,Main	AEX73878201	LGA290.ABRAZY BK:Black -	
2	MEZ002100	Label,Approval	MEZ64403301	COMPLEX LGA290.ABRASV ZZ:Without Color -	

Level	LocationNo.	Description	PartNumber	Spec	Remark
1	AGF000000	Package Assembly	AGF76407301	LGA290.ABRASV ZZ:Without Color LGA290 BRA(Brazil Package)	
1	AAD000000	Addition Assembly	AAD85994601	LGA290.ABRASV ZY:Color Unfixed -	

12.2 ReplacementParts <Main component>

Note: This Chapterisused for reference, Part order is ordered by SBOM standard on GCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
3	EBR00	PCB Assembly,Main	EBR74262801	LGA290.ABRAZY 1.0 Main	
4	EBR071500	PCB Assembly Main,Insert	EBR74606301	LGA290.ABRAZY 1.0 Main	
5	SJMY00	Motor,DC	SJMY0007104	3V 80mA 0A 12KRPM 0RPM 0SEC 0GF.CM 0OHM	
5	RAA050100	Resin,PC	BRAH0001301	UF2040 or 3075BHF . . NONE	
5	EAB00	Speaker,Dual Mode	EAB62308201	1812-8T-04W2P Nd-Fe-B 700mW 8OHM 91DB 720HZ 1812*3.0T wire 15mm DCCA coil WIRE KIRYN TELECOM CO., LTD	
5	EAJ00	LCD Module	EAJ62010101	GPM1233A1 QCIF 2.2INCH 176X220 350CD COLOR 50% 4/3 400:1 120Hz Inverter N - - 39.85x52.95x1.9t, ILI9225G-S (ILITEK) GIANTPLUS TECHNOLOGY CO., LTD.	
5	EBP00	Camera Module	EBP61322001	CW1334-ABDBS CW1334-ABDBS 1.3M hynix 1/6 COWELL ELECTRONICS CO.,LTD	
4	EBR071800	PCB Assembly Main,SMT	EBR74262901	LGA290.ABRAZY 1.0 Main	
5	SAD010000	Software,Mobile	SAD33240401	Base V10b - BRAZIL MTK -	
5	EBR071600	PCB Assembly Main,SMT Bottom	EBR74263001	LGA290.ABRAZY 1.2 Main	
6	Q200	FET	EQFP0007601	KTJ6131E P-CHANNEL MOSFET -30V +-20 -0.05A 20OHM 100mW ESM R/TP 3P KEC CORPORAITION	
6	R412	Resistor,Chip	ERHZ0000221	MCR01MZP5F1502 15KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	C268	Capacitor Ceramic,Chip	ECZH0003118	GRM155R71H561K 560pF 10% 50V X7R - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C303	Capacitor,TA Conformal	EAE62287901	251M1002107MR12A168 100uF 20% 10V 50UA -55TO+125C 0.6OHM 3.2X1.6X1.1MM NONE SMD R/TP 1.2T max. MATSUO ELECTRIC CO.,LTD	
6	VA206 VA207	Varistor	SEVY0007301	ULCE0505C015FR 5V 0% 0.5F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	L400	Inductor Multilayer,Chip	ELCH0003828	LQG15HS2N4S02D 2.4NH 0.3NH - 300mA 0.15OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	ZD300	Diode,Zener	EAH61793901	KDZ5.1EV-RTK/P 5.2V 4.98TO5.2V 70OHM 150mW ESC R/TP 2P 1 KEC CORPORAITION	
6	R256	Resistor,Chip	ERHZ0000434	MCR01MZP5J1R0 1OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C408	Capacitor Ceramic,Chip	ECCH0000105	MCH155A040C 4pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	FB204 FB206	Resistor,Chip	ERHZ0000401	MCR01MZSJ000 0OHM 5% 1/16W 1005 R/TP - ROHM.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C118 C120 C121 C123 C125 C126 C128 C129 C130 C131 C132 C133 C134 C136 C204 C205 C235 C238 C240 C241 C242 C243 C244 C245 C247 C254 C257 C258 C259 C265 C270 C308 C309 C310	Capacitor Ceramic,Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	C318 C320 C322 C425 C426 C427 C429 C433 C435	Capacitor Ceramic,Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	C108 C135 C201 C206 C211 C223 C225 C228 C230	Capacitor Ceramic,Chip	ECZH0003103	GRM36X7R104K10PT 100nF 10% 10V X7R - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	R410	Resistor,Chip	ERHZ0000483	MCR01MZP5J470 47OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R250	Resistor,Chip	ERHZ0000484	MCR01MZP5J471 470OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C266 C267 C269 C271 C434	Capacitor Ceramic,Chip	ECCH0000143	MCH155CN102KK 1nF 10% 50V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	FL300 FL301 FL302 FL303 FL304	Filter,EMI/Power	SFEY0011401	ICVE10184E070R101FR ESD/EMI 0HZ 7.5pF 0H SMD R/TP INNOCHIPS TECHNOLOGY	
6	C417 C418 C419 C420 C436	Capacitor Ceramic,Chip	ECCH0000113	MCH155A180J 18pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R101 R103 R117 R201 R308 R310 R311	Resistor,Chip	ERHZ0000406	MCR01MZP5J104 100KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	VA101 VA102 VA103 VA104 VA200 VA201 VA203 VA204 VA224 VA225, VA226 VA302 VA303 VA305 VA306 VA308 VA309 VA311 VA314 VA315	Varistor	SEVY0005402	ICVS0505500FR 5.6V 0% 50F 1.0*0.5*0.55 - SMD R/TP INNOCHIPS TECHNOLOGY	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	U100	IC,MCP,NOR	EAN62212601	PF38F5060M0Y3DK NOR/512 PSRAM/128 1.7VTO2V,1.7VTO1.95V 8.0*8.0*1.0 TR 56P NOR+PSRAM BGA 512Mbit(MICRON 65nm,AAD MUX)+128Mbit(WINBOND 65nm,AD MUX) MICRON SEMICONDUCTOR ASIA PTE LTD.	
6	R100 R113 R241 R247 R248 R312 R415	PCB ASSY,MAIN,PAD SHORT	SAFP0000401	LG-LU3000 LGTBK,MAIN,A,	
6	R104 R105 R106 R107 R109 R110 R218 R219 R223 R227 R233	Resistor,Chip	ERHZ0000443	MCR01MZP5J222 2.2KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C109 C127	Capacitor Ceramic,Chip	ECCH0017601	CL05A475MQ5NRNC 4.7uF 20% 6.3V X5R -55TO+85C 1005 R/TP 0.5MM SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	FB104 FB300	Filter,Bead	SFBH0007103	BLM15BB750SN1D 75 ohm 1.0X0.5X0.5 25% 0.4 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO.,LTD.	
6	C212 C213	Capacitor Ceramic,Chip	ECZH0000841	C1005C0G1H560JT000F 56pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C203 C214 C217 C218 C219 C226	Capacitor Ceramic,Chip	ECCH0000198	CL05A225MQ5NSNC 2.2uF 20% 6.3V X5R -55TO+85C 1005 R/TP . SAMSUNG ELECTRO-MECHANICS CO., LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C106 C107 C110 C112 C140 C234 C307 C315 C316 C317	Capacitor Ceramic,Chip	ECCH0004904	GRM155R60J105K 1uF 10% 6.3V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	R116 R216 R251 R320	Resistor,Chip	ERHZ0000404	MCR01MZP5J102 1KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C312 C313	Capacitor Ceramic,Chip	ECCH0010501	GRM1555C1H7R5D 7.5pF 0.5PF 50V C0G - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	R301 R302 R303 R304 R305 R306 R309 R316 R317 R318	Resistor,Chip	ERHZ0000505	MCR01MZP5J681 680OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R221 R226 R232	Resistor,Chip	ERHZ0000486	MCR01MZP5J473 47KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R204	Resistor,Chip	ERHZ0000402	MCR01MZP5J100 10OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C215 C216 C224 C302 C304	Capacitor Ceramic,Chip	ECCH0000120	MCH155A390J 39pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	L411	Inductor Multilayer,Chip	ELCH0004715	1005GC2T27NJLF 27NH 5% - 200mA 0.9OHM 1.4GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	C122 C421 C422	Capacitor Ceramic,Chip	ECCH0000185	GRM1555C1H5R6C 5.6pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C124 C222	Capacitor Ceramic,Chip	ECCH0005604	GRM188R60J106M 10000000 pF,6.3V,M,X5R,TC,1608,R/TP,0.8 mm MURATA MANUFACTURING CO.,LTD.	
6	C103 C105 C229	Capacitor Ceramic,Chip	ECCH0000122	MCH155A470JK 47pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	FB201 FB202	Filter,Bead	EAM62072101	BLM15PD600SN1D 60 ohm 1.0x0.5x0.5 25% 0.06 ohm 1.1A SMD R/TP 2P 0 MURATA MANUFACTURING CO.,LTD.	
6	S200	Socket,Card	ENSY0018601	49448-1611 Micro-SD 8P STRAIGHT SMD R/TP Combo MOLEX JAPAN CO.,LTD.	
6	R217	Resistor,Chip	ERHZ0000529	MCR01MZP5J152 1.5KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C405 C411 C412 C428	Capacitor Ceramic,Chip	ECZH0000813	C1005C0G1H101JT 100pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	U101	IC,Digital Baseband Processor,GSM	EUSY0409701	MT6253 0 0 0 NONE NONE 263P - BGA R/TP 263P MEDIATEK SINGAPORE PTE.LTD.	
6	C111 C113 C114 C115 C116 C117 C141	Capacitor Ceramic,Chip	ECZH0004402	CL05F104ZO5NNNC 0.1uF -20TO+80% 16V Y5V -30TO+85C 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R314 R315	Resistor,Chip	ERHZ0000206	MCR01MZP5F10R0 10OHM 1% 1/16W 1005 R/TP - ROHM.	
6	C321	Capacitor Ceramic,Chip	ECZH0001107	C1005X7R1E562KT000F 5.6nF 10% 25V X7R -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	R114	Resistor,Chip	ERHZ0000499	MCR01MZP5J562 5.6KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	U200	IC,Audio Sub System	EUSY0420001	TPA2055D3 1.6~5.5V 0W WLCSP R/TP 20P - TEXAS INSTRUMENTS INCO.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	VA209 VA210 VA211 VA212 VA213 VA214 VA215 VA216 VA217 VA218 VA219 VA220 VA221 VA222 VA223	Varistor	SEVY0004301	ICVL0518100Y500FR 18V 0% 10F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	FB100 FB101 FB105 FB200 FB207 FB210 FB211	Filter,Bead	SFBH0008105	BLM15BD182SN1D 1800 ohm 1.0X0.5X0.5 25% 1.4 ohm 0.1A SMD R/TP 2P 0 MURATA MANUFACTURING CO.,LTD.	
6	R102	Resistor,Chip	ERHZ0000294	MCR01MZP5F5101 5.1KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	C263	Capacitor Ceramic,Chip	ECZH0000810	C1005C0G1H090DT000F 9pF 0.5PF 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	L401 L403	Inductor Multilayer,Chip	ELCH0003839	LQG15HS22NJ02D 22NH 5% - 300mA 0.42OHM 1.9GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	R313	Resistor,Chip	ERHY0000181	RC1005F150CS 15OHM 1% 1/16W 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	FL400	Filter,Saw,Dual	SFSB0002305	B9512 881.5MHz, 942.5MHz 1.8*1.4*0.68 SMD R/TP 10P EPCOS PTE LTD.	
6	R413	Resistor,Chip	ERHZ0000204	MCR01MZP5F1003 100KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	FL401	Filter,Saw,Dual	SFSB0002306	B9513 1805M~1880M, 1930M~1990M 1.8*1.4*0.68 SMD R/TP 10P EPCOS PTE LTD.	
6	CN302	Connector,BtoB	ENBY0034201	GB042-24S-H10-E3000 24P 0.40MM STRAIGHT SOCKET SMD R/TP 1M - LS Mtron Ltd.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	FL402	Filter,Ceramic	SFCY0000901	LFB212G45SG8A166 BPF 2.45KHZ 100Hz SMD R/TP 4P MURATA MANUFACTURING CO.,LTD.	
6	R208 R209	Resistor,Chip	ERHZ0000545	MCR01MZSJ5R6 5.6OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R206 R207	Resistor,Chip	ERHZ0000348	MCR01MZP5F12R0 12OHM 1% 1/16W 1005 R/TP - ROHM.	
6	C119 C410	Capacitor Ceramic,Chip	ECCH0007803	CL10A106MP8NNNC 10uF 20% 10V X5R - 55TO+85C 1608 R/TP 0.8MM SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R300	Resistor,Chip	ERHZ0000252	MCR01MZP5F2403 240KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	C200 C237 C239 C305	Capacitor Ceramic,Chip	ECCH0007804	CL05A225MP5NSNC 2.2uF 20% 10V X5R - 55TO+85C 1005 R/TP 0.5MM SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	U202	IC,Multiplexer	EAN62228101	MT6306 3.2~4.3V 999 ANALOG SWITCH/MULTIPLEXER QFN R/TP 28P SIM Controller MEDIATEK INC.	
6	C306 C401	Capacitor Ceramic,Chip	ECZH0000830	C1005C0G1H330JT000F 33pF 5% 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	CN301	Connector,FFC/FPC/PIC	ENQY0013901	04-6293-635-005-829+ 35P 0.30MM FPC ANGLE BOTH SMD R/TP LOCKING FLIP TYPE KYOCERA ELCO KOREA SALES CO.,LTD.	
6	R220 R222 R254 R255	Resistor,Chip	ERHZ0000513	MCR01MZP5J821 820OHM 5% 1/16W 1005 R/TP - ROHM.	
6	U203	IC,Mini ABB	EAN62227701	SNB1058A0RSMR Mini ABB : MUIC, Charger IC, Current Sink, LDOs QFN R/TP 32P TEXAS INSTRUMENTS KOREA LTD, HONGKONG BRANCH.	
6	C138 C233 C236	Capacitor Ceramic,Chip	ECCH0000115	MCH155A220JK 22pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C137	Capacitor Ceramic,Chip	ECCH0000117	CL05C270JB5NNNC 27pF 5% 50V NP0 - 55TO+125C 1005 R/TP 0.5 SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R200	Resistor,Chip	ERHZ0000407	MCR01MZP5J105 1MOHM 5% 1/16W 1005 R/TP - ROHM.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	L402	Inductor Multilayer,Chip	ELCH0003818	LQG15HS9N1J02D 9.1NH 5% - 300mA 0.26OHM 3.4GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	C415	Capacitor Ceramic,Chip	ECZH0001002	C1005CH1H0R5BT000F 0.5pF 0.1PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C423 C424	Capacitor Ceramic,Chip	ECCH0001001	C1005C0G1H6R8CT000F 6.8pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	CN201	Connector,I/O	ENRY0008801	GU073-5P-SD-E1500 GU073-5P-SD-E1500,5,mm,ANGLE LS Mtron Ltd.	
6	X101	Crystal	EXXY0018701	FC-135(12.5PF, +-20PPM) 32.768KHZ 20PPM 12.5PF 32*15 SMD R/TP SEIKO EPSON CORP	
6	SW400	Connector,RF	ENWY0008701	MS-156C NONE STRAIGHT SOCKET SMD T/REEL AU 50OHM 400mDB HIROSE KOREA CO.,LTD	
6	C403 R108 R402	Resistor,Chip	ERHY0000105	MCR01MZP5F51R0 51OHM 1% 1/16W 1005 R/TP - ROHM.	
6	X100	Crystal	EXXY0027401	X1E000021043400 26MHZ 10PPM 0F NONE SMD R/TP EPSON TOYOCOM CORP	
6	C431	Capacitor Ceramic,Chip	EAE62563601	C1005NP0159CGTQ 1.5pF 0.25PF 50V C0G - 55TO+125C 1005 R/TP 0.55T max. DARFON ELECTRONICS CORP.	
6	R409	Resistor,Chip	ERHZ0000449	MCR01MZP5J243 24KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	J201,J202	Card Socket	EAG63032701	5000-6P-1.8SLB SIM 6P STRAIGHT SMD R/TP - HYUPJIN I&C CO.,LTD.	
6	L405	Inductor Multilayer,Chip	ELCH0003834	LQG15HS4N3S02D 4.3NH 0.3NH - 300mA 0.18OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	BAT100	Capacitor Assembly	SMZY0023501	PAS311HR-VG1 3.8 Backup Capacitor 0.03F,Module Assembly, KOREA TAIYO YUDEN.CO., LTD.	
6	CN300	Connector,Terminal Block	EAG62810901	KQ03LV1-3R 3P 2.50MM ANGLE SMD T/REEL NEMO HIROSE ELECTRIC CO., LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	L100	Inductor,Wire Wound,Chip	ELCP0008017	CIG21L2R2MNE 2.2UH 20% - 500mA 0.5 0.95 0.16OHM - - SHIELD 2X1.25X1MM NONE R/TP SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	U401	IC,Bluetooth	EAN62212501	MT6626P/A-L BT2.1 EDR, FM Radio(RDS), 3.06x2.56x0.53, 110nm, 0.4pitch WLCSP R/TP 40P MEDIATEK INC.	
6	U400	Module,Tx Module	SMRH0007101	SKY77550 33DBM,33DBM,31DBM,31DBM 30DB,30DB,28DB,28DB 39%,39%,37%,37% 50UA 1.46A,970mA -33DB,-33DB -45DBM -1.3DBM 28P 6.0x6.0x1.0MM - SKYWORKS SOLUTIONS INC.	
6	C407	Capacitor Ceramic,Chip	ECCH0000133	C1005X7R1H221KT000F 0.22nF 10% 50V X7R - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	EAB01	Microphone Condenser	EAB62291401	SOB410S44VRC 44DB 2.2KOHM OMNI 1.5TO4V 4pi 1.2t SMD BSE CO., LTD.	
6	SW300	Switch,Tact	ESCY0004401	LS12K2-T NONE 12VDC 0.02A HORIZONTAL 0GF T/REEL - CITIZEN ELECTRONICS CO.,LTD.	
6	VA205	Varistor	SEVY0005202	EVLC5S02100 5.5V 0% 100F 1.0*0.5*0.6 UL SMD R/TP AMOTECH CO., LTD.	
6	C252	Capacitor Ceramic,Chip	ECCH0000155	MCH153CN103KK 10nF 10% 16V X7R - 55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	LD306	LED,Chip	EDLH0015202	99-216UTC/TR8-1 WHITE 2.95~3.3 30mA 1440~1720mcd x, y 110mW - R/TP 2P - EVERLIGHT ELECTRONICS CO., LTD.	
6	L406	Inductor Multilayer,Chip	ELCH0001054	1005GC2T5N6SLF 5.6NH 0.3NH - 300mA 0.27OHM 3.2GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	C250	Capacitor Ceramic,Chip	EAE62505701	CL10A105KB8NNNC 1uF 10% 50V X5R - 55TO+85C 1608 R/TP 0.9T max. SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	FB102	Filter,Bead	SFBH0008101	BLM15AG601SN1D 600 ohm 1.0X0.5X0.5 25% 0.6 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO.,LTD.	
6	VA100	Varistor	SEVY0003601	ICVL0505101V150FR 5.6V 0% 60F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	J200	Jack,Phone	EAG63010701	KJA-PH-0-0183 4P 4P ANGLE R/TP 3.5M BLACK 5P Reverse shape KSD CO., LTD	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	L404	Inductor Multilayer,Chip	ELCH0003835	LQG15HS4N7S02D 4.7NH 0.3NH - 300mA 0.18OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	C202	Capacitor Ceramic,Chip	ECCH0000109	MCH155A080DK 8pF 0.5PF 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R407	Resistor,Chip	ERHZ0000405	MCR01MZP5J103 10KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	L200	Inductor Multilayer,Chip	ELCH0010402	LK1005 R27K-T 270NH 10% - 25mA - - 1.2OHM 120MHZ 10 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO.,LTD	
6	FB209	Filter,Bead	SFBH0007101	BLM15AG121SN1D 120 ohm 1.0X0.5X0.5 25% 0.25 ohm 0.5A SMD R/TP 2P 0 MURATA MANUFACTURING CO.,LTD.	
5	EBR071700	PCB Assembly,Main SMT Top	EBR74263101	LGA290.ABRAZY 1.0 Main	
6	EAX010000	PCB,Main	EAX64452001	LGA290.ABRAZY 1.1 FR-4 SBL 6 0.8 Main	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C118 C120 C121 C123 C125 C126 C128 C129 C130 C131 C132 C133 C134 C136 C204 C205 C235 C238 C240 C241 C242 C243 C244 C245 C247 C254 C257 C258 C259 C265 C270 C308 C309 C310	Capacitor Ceramic,Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	C318 C320 C322 C425 C426 C427 C429 C433 C435	Capacitor Ceramic,Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	LD300 LD301 LD302 LD303 LD304 LD305	LED,Chip	EDLH0015101	19-217/BHC-ZM1N2QY/3T BLUE 2.7~3.2 25mA 18~45mcd 465~475nm 95mW 1608 R/TP 2P - EVERLIGHT ELECTRONICS CO., LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	VA101 VA102 VA103 VA104 VA200 VA201 VA203 VA204 VA224 VA225 VA226 VA302 VA303 VA305 VA306 VA308 VA309 VA311 VA314 VA315	Varistor	SEVY0005402	ICVS0505500FR 5.6V 0% 50F 1.0*0.5*0.55 - SMD R/TP INNOCHIPS TECHNOLOGY	
4	EAA00	PIFA Antenna,Multiple	EAA62764501	KI-M08720 QUAD -2DB 5 Metal Stamping Type - KOMATECH CO.,LTD	

12.3 Accessory

Note: This Chapterisused for reference,Part order is ordered by SBOM standard onGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
2	EBX000000	Accessory,Data Cable	SGDY0017902	LG0038 ,1.2M,BLACK, ningbo broad telecommunication co.,ltd	
2	EAB010200	Earphone,Stereo	SGEY0003219	EMB-LGE001STKE ,BLACK,4 POLE PLUG,3.5 4,Earphone,Stereo CRESYN CO.,LTD	
2	EAY060000	Adapters	SSAD0036504	STA-U34BS 90Vac~264Vac 5.1V 700mA 5060 CE NONE NONE - SALCOMP OY	
2	EAN011400	IC,Memory Card,MICRO SD	EAN62171601	SD-C02G2CYB(LQBKP) 2GBYTE 2.7VTO3.6V MICRO SD CARD 15.0x11.0x1.0MM TR 8P 2GB MicroSD Card (32nm TLC) TOSHIBA ELECTRONICS KOREA CORPORATION	
2	MCK00	Cover,Battery	MCK67064501	MOLD PC LGA290.ABRAZY SF:SILVER BLACK -	
2	EAC00	Rechargeable Battery Lithium Ion	EAC61679601	BL-44JN-WWU-LGC PRISMATIC 3.7V 1.5AH 300mAH 61x44x4.4 65x44x4.8 BLACK Bar type, Top cap Screw joint 444461, 1500mAh, Bar Type (Top cap screw joint), WW, Up LG Chem,LTD.	
2	MFL053800	Manual,Operation	MFL67450001	COMPLEX LGA290.ABRASV ZZ:Without Color Full manual for LG290 ABRA	